Titre: Title:	A computer controlled passive multi-harmonic tuner used to optimise a power fet up to the third harmonic
Auteur: Author:	Cornelius Viereck
Date:	1998
Type:	Mémoire ou thèse / Dissertation or Thesis
Référence: Citation:	Viereck, C. (1998). A computer controlled passive multi-harmonic tuner used to optimise a power fet up to the third harmonic [Mémoire de maîtrise, École Polytechnique de Montréal]. PolyPublie. https://publications.polymtl.ca/8562/

UNIVERSITÉ DE MONTRÉAL

A COMPUTER CONTROLLED PASSIVE MULTI-HARMONIC TUNER USED TO OPTIMISE A POWER FET UP TO THE THIRD HARMONIC

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MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION
DU DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES
(GÉNIE ÉLECTRIQUE)

Décembre 1998

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Ce mémoire intitulé:

A COMPUTER CONTROLLED PASSIVE MULTI-HARMONIC TUNER USED TO OPTIMISE A POWER FET UP TO THE THIRD HARMONIC

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en vue de l'obtention du diplôme de: Maîtrise ès sciences appliquées
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To my mother and father

Acknowledgements

I would like to thank my director, Prof Renato Bosisio for accepting my will to learn more about high frequency testing and for putting me in contact with Focus Microwaves and for supporting my work in this project, as well as my endeavours into bicycle racing.

I would also like to thank my co-director Dr. Christos Tsironis, president and head researcher at Focus Microwaves, who allowed me full usage of his facilities, and who always encouraged full blown hedonistic research and development of microwave technology.

Acknowledgement must go out to Dominique Dubouil, talented researcher at Focus Microwaves, for the quick, correct and concise help he always gave me.

Also to Camille Ghali and François Allard of the same company for their technical contributions and amiable support.

Thank-you to Fujitsu in Sunnyvale California for supplying the transistors.

Abstract

A passive multi-harmonic tuner within an automated passive load pull system is evaluated. Only the phase of the second and third harmonics are adjusted by this serial harmonic tuning device which presents an almost constant reflection factor of up to 0.95 to these harmonic components. The multi-harmonic tuner is tuned to the second and third harmonic of the fundamental which in this case was the PCS frequency of 1.8GHz. No power splitters, combiners, doublers, or extra filters are used in this relatively simple hardware setup. The host system software handles the calibration, tuning and S-parameter manipulations.

Since the two harmonic resonators are in series, and in front of, the fundamental tuner, the system must stabilise the fundamental impedance by readjusting the fundamental tuner impedance each time a harmonic resonator is moved. This is because the harmonic resonators modify the fundamental impedance a small amount as they move because they do present a small reflection to the fundamental signal. Measurements are taken with and without the correction facility enabled to be able to visualize the impedance stability, and would be deviation, during each harmonic sweep.

The subject of load pull and load pull system architecture is described for systems in general and to this system in particular. The fundamental load pull setup was calibrated and then this calibration was verified using only a "through line". S-parameter measurements are presented which were performed on the stand alone multi-harmonic tuner with a network analyser. Then the fundamental and multi-harmonic tuners are connected together and measured on the network analyser and in the setup to verify that the impedances are stable during first (fundamental) second and third harmonic sweeps.

It was found that the system performed well even if some areas of instability did exist, which depended on the angles and magnitudes of the reflection coefficients of the three harmonics. Certain angles and magnitudes of the fundamental impedance were especially prone to instability during harmonic sweeps. These had reflection coefficients higher than 0.8 and angles where a harmonic resonator presented a larger than usual reflection at the fundamental, or a larger than usual change in the reflection, during sweeps which rendered the intended fundamental impedance sensitive to harmonic resonator movement. These problems gave rise to ideas for improving this promising tuning device.

In view of this, a fundamental impedance was chosen which was relatively insensitive to changes during harmonic sweeps, and which optimised the power/efficiency performance of a 3W GaAs MESFET being tested. The DC bias point placed the device in the class AB mode. A discussion on load lines and amplifier classes ensues. Load and source pull results at seven DC bias points are presented. The centre frequency was 1.8GHz and two band edge frequencies of 1.75GHz and 1.85GHz, representing a 100MHz bandwidth, are also measured and presented.

This impedance had a magnitude of reflection of 0.6, which was 0.1 below the optimum for this device. The magnitude was also chosen to be able to accommodate the multi-harmonic tuner which, when placed between the fundamental tuner and the device under test, lowers the maximum attainable reflection coefficient at the fundamental to about 0.7 due to its (nonetheless small) insertion loss. This extra "room to move" is needed to ensure that proper impedance corrections take place during harmonic sweeps.

Harmonic optimisation at the centre frequency increased the output power by 0.5dBm and the efficiency by 9% for 1dB compression. The accuracy remained good at 1.85GHz, yielding a 0.4dBm and 4%

performance improvement. Insertion losses proved too high at 1.75GHz. It was difficult, at this stage of development of the multi-harmonic tuner, to establish how much of this improvement was due to the second and third harmonic, respectively.

Résumé

Un nouveau synthétiseur passif à multi-harmoniques, installé dans un système existant de load pull passif automatisé, est évalué. Seulement la phase de la deuxième et la troisième harmonique est ajustable par cet instrument qui présente à ces harmoniques un coefficient de réflexion jusqu'à 0.95. Le synthétiseur multi-harmoniques est ajusté à la deuxième et à la troisième harmonique de la (fréquence) fondamentale qui est, dans ce cas, la fréquence SCP de 1.85GHz. Aucun diviseur de puissance, combineur, doubleur, triplexeur ou filtre externe ne sont utilisés dans ce montage qui est relativement simple. La calibration, la synthétisation et la manipulation des paramètres-S sont effectuées par le logiciel à partir du système hôte.

Vu que les deux résonateurs harmoniques sont en série et devant le synthétiseur fondamental, le système doit stabiliser l'impédance fondamentale en re-ajustant l'impédance à chaque fois que les résonateurs harmoniques bougent. La raison de ceci est que les résonateurs harmoniques modifient un peu l'impédance de la fondamentale à cause de la réflexion résiduelle au signal fondamental. Des résultats sont présentés avec la fonction de correction d'impédance appliquée (ou pas) pour visualiser la stabilité (ou la déviation) de l'impédance fondamentale durant le balayage harmonique.

L'architecture et l'opération des systèmes de load pull sont décrites généralement et spécifiquement pour le système proposé. Le système de load pull fondamental est calibré et cette calibration est vérifiée en utilisant une technique de "through line". Les mesures des paramètres-S sont effectuées sur le synthétiseur multi-harmoniques avec un analyseur de réseau. Les synthétiseurs (fondamental et multi-harmonique) sont connectés ensemble et mesurés sur un analyseur de réseau pour mesurer les impédances durant le

balayage de la première (fondamental), deuxième, et troisième harmonique.

Il a été constaté qu'il y avait des régions d'instabilité dépendant des angles et amplitudes de la réflexion à chaque harmonique. Certaines impédances aux fondamentales étaient moins stables pendant les balayages effectués avec le synthétiseur multi-harmonique. Ces impédances fondamentales avaient une amplitude de coefficient de réflexion plus important que 0.8 ou un angle de réflexion qui la situait dans un endroit sur l'abaque de Smith où le résonateur harmonique avait une plus grande réflexion à la fondamentale ou un plus grand changement de l'impédance à la fondamentale. Ces problèmes donnaient des inspirations pour trouver les méthodes pour améliorer ce synthétiseur utile.

Une impédance qui était un bon compromis entre la stabilité à la fondamentale et l'optimisation de la puissance et l'efficacité d'un FET de 3W a été choisie. Le point de polarisation le plaçait dans la class AB. Les résultats du source pull et load pull à sept points de polarisation sont présentés. La fréquence centrale est de 1.8GHz. La performance a été aussi mesurée à 1.75GHz et à 1.85GHz, ce qui représente une largeur de bande de 100MHz.

L'impédance choisie avait une amplitude de coefficient de réflexion de 0.6, qui était 0.1 en bas de l'optimum pour ce dispositif. Cette amplitude a aussi été choisie pour accommoder le synthétiseur multi-harmoniques qui diminue le coefficient de réflexion maximale à la fondamentale quand placé entre le synthétiseur fondamental et le dispositif dû à sa perte d'insertion. La diminution de l'amplitude du coefficient de réflexion est aussi nécessaire pour accommoder la fonction de correction de l'impédance fondamentale durant les balayages harmoniques.

L'optimisation harmonique à la fondamentale a augmenté la puissance de sortie de 0.5dBm et l'efficacité de 9%, avec une

puissance de sortie de 0.5dBm et l'efficacité de 9%, avec une compression de 1dB. L'optimisation est restée favorable à 1.85GHz, avec une amélioration de 0.4dBm et 4%. Les pertes d'insertion étaient trop élevées à 1.75GHz. Il a été difficile de constater la contribution de la deuxième ainsi que de la troisième impédance harmonique à cette amélioration.

CONDENSÉ EN FRANÇAIS

The following is a condensed version of the entire work in french.

The table of contents appears on page xxviii (28).

Chapitre 1
Les Systèmes de Load Pull Fondamental et Harmonique

1.1 - Général

Le "load pull" est une technique de mesure où un paramètre à la sortie d'un dispositif est mesuré (typiquement la puissance) pendant que la charge est variée. Ceci donne la relation entre la puissance et l'impédance de sortie, à une fréquence et un point de polarisation spécifique. Une partie du signal est retournée au dispositif avec son amplitude et sa phase modifiée, qui réagi avec l'onde qui part du dispositif, et modifie l'opération du dispositif d'une certaine manière.

Le banc de mesure de Load pull est surtout utilisé pour étudier la sortie des transistors qui opèrent dans un mode de grand signal (où les harmoniques sont générées). Les résultats sont utilisés pour la conception des amplificateurs, la vérification des modèles des logiciels, et pour vérifier les spécifications données par les manufacturiers.

Le "source pull" peut aussi être effectué sur un dispositif. Dans ce cas, un paramètre de sortie est mesuré pendant que l'impédance de source est variée par un synthétiseur connecté à l'entrée.

Un système classique de load pull passif est montré dans la figure 1.1. L'impédance des synthétiseurs à l'entrée et à la sortie

peut être obtenue par les coefficients de réflexions mesurées avec les coupleurs bi-directionnele. Sans les coupleurs, les synthétiseurs doivent être déconnectés et mesurés sur un analyseur de réseau. Cette manipulation est inconvenable, donc la méthode de déduire l'impédance des synthétiseurs pendant qu'ils sont dans le circuit est préféré.

Si le niveau de gain est maximisé, en cherchant l'impédance à l'entrée qui donne la plus haute puissance à la sortie (source pull sans compression), l'adaptation à l'entrée sera maximisée. Dans ce cas G_A est maximisé et $P_{in}=P_{AVS}$. Un puissance mètre à deux canaux sera suffisant comme dans le montage proposé et montré dans la figure 2.1. Vû qu'il y a seulement un détecteur de puissance à l'entrée, les valeurs de G_A ne sont pas mesurables. Ceci n'est pas un problème dans un système qui a le but d'optimiser les amplificateurs de puissance. Ils sont toujours adaptés à l'entrée. Les paramètres d'intérêt sont à la sortie. C'est G_T qui est actuellement mesuré avec deux détecteurs de puissances comme montré à la figure 2.1. Une adaptation d'entrée (return loss) de 25dB est normale dans un montage de load pull[2], donc $G_p=G_T$.

1.2 - Load Pull Actif

Dans un système de load pull actif, une charge virtuelle est présentée au DST (Dispositif Sous Test). Un signal synchronisé avec celui qui passe dans le DST est injecté vers la sortie. L'avantage c'est un balayage plus complet sur l'abaque. Le désavantage c'est que le montage à une plus grande complexité. Il y a deux topologies majeures : Takayama et "one port load", montrées dans la figure 1.4 et 1.5.

1.3 - Load Pull Harmonique

Le gain en performance obtenu avec le tuning harmonique est plus important pendant l'opération non linéaire du transistor. Le but est de récupérer l'énergie des harmoniques et de le "recycler" pour: a)augmenter l'énergie du signal fondamental qui augmentera la puissance désirée et b)réduire l'énergie d'alimentation ce qui augmentera l'efficacité.

Les gains de puissances dûs à l'optimisation de la deuxième harmonique sont reportés de 0.4dB [4] à 1.5dB [7]. Les gains d'efficacité ajoutés (PAE) sont reportés de 4.1% [4] à 12% [7]. Les gains reportés pour l'optimisation de la troisième harmonique sont moins définis.

L'augmentation de l'efficacité est dûe à la diminution de la dissipation de puissance dans le dispositif. Pour l'augmentation de puissance, il est possible qu'il y ait un effet de mélangeur entre l'harmonique et la fondamentale. L'étude de ce mécanisme n'est pas l'objectif de ce mémoire.

Pour récupérer l'énergie d'une harmonique il faut que le maximum de puissance de l'harmonique soit retourné au dispositif. C'est la phase d'une harmonique bien reflétée qui doit être optimisée. Mais, plus élevée est la réflexion d'une harmonique le plus important il est de l'optimiser, parce que la performance peut aussi diminuer [4].

Certains bancs de mesure de load pull à la fondamentale présentent aux harmoniques une impédance autres que 50Ω. Ceci cause qu'une impédance "fondamentale" peut être choisie partiellement aux effets des impédances aux harmoniques. Un banc de mesure de load pull harmonique essaie de séparer les effets de chaque harmonique

pour qu'ils n'aient pas un effet l'un sûr l'autre.

La figure 1.6 montre une approche inédite pour synthétiser et ajuster les impédances harmoniques [9]. Les feuilles d'or, d'un quart d'onde de l'harmonique voulue, sont placées sur le substrat à l'endroit où la phase de l'harmonique est optimisée. Les avantages de cette topologie est que 1) les "stubs" ne présentents aucune partie réelle (aucune pertes) à la fondamentale, donc sa capacité de tuning est conservée, 2) la réflexion aux harmoniques est haute, dû à la proximité des "stubs" et 3) ce n'est plus nécessaire que le synthétiseur fondamental soit à bande étroite à cause que les harmoniques sont déjà reflétées vers le dispositif 4)vu que c'est une topologie proche à la conception finale, il y aura moins de possibilitées d'avoir des différences de performance [10].

Le synthétiseur multi-harmoniques est basé sur ce concept.

Chapitre 2

Le Système de Load Pull Passif Automatisé

2.1 - Introduction

Le montage du système est montré à la figure 2.1. Il a été développé par la companie "Focus Microwaves" à Montréal. Après la calibration de chaque composante, il n'est plus nécessaire de déconnecter le montage. Les impédances sont connues des endroits divers, pour chaque position du synthétiseur. Les instruments sont connectés sur un réseau de GPIB. Une abaque de Smith est typiquement montrée sur l'écran avec les impédances de l'entrée, Γ_s, et l'impédance de la sortie, Γ_L, montrées.

2.2 - Les Synthétiseurs Fondamentaux Automatisés

Les facteurs qui s'appliquent sur les synthétiseurs manuels s'appliquent aussi sur ceux-ci. Les deux moteurs avec ses circuits de contrôle, un pour la direction "x" et l'autre pour la direction "y", et l'interface, permet de les contrôler par ordinateur.

2.3 - La Calibration

Toutes les composantes doivent être caractérisés. L'analyseur de réseau doit être bien calibré avant la caractérisation des composants, surtout pour les synthétiseurs qui présentent les très hautes réflexions. Il est bien établi que la méthode TRL est la meilleure technique à utiliser pour calibrer l'analyseur. Les blocs du montage sont calibrés séparément sur l'analyseur sous le contrôle de l'ordinateur hôte. Il y a un bloc d'entrée, un bloc de sortie, et fixture de test. Le fixture de test est calibré avec la méthode TRL aussi.

2.4 - Changer les Plans de Références

S_{11} en regardant de la sortie du DST doit être connu avant que l'impédance de sortie puisse être trouvée. Pour changer la référence du synthétiseur à la sortie du dispositif les paramètres-S du bloc de la sortie, le synthétiseur, et la deuxième partie du fixture de test sont cascadés. Voir la figure 2.2 et les équations 2.1 à 2.7.

2.5 - Les mesures et calculs de puissances

La puissance du dispositif est calculée comme montré aux équations 2.8 et 2.9.

Chapitre 3
Le Synthétiseur Multi-harmonique et le Système de Load Pull Multi-harmonique.

3.1 - Introduction

Le synthétiseur multi-harmonique est installé entre le DST et le synthétiseur fondamental. Le concept est comme décrit à la fin de la section 1.3.

3.2 - Le synthétiseur multi-harmonique

Les figures 3.2 et 3.3 montrent les balayages d'impédances à l'entrée du synthétiseur pour la deuxième et troisième harmonique. Les figures 3.4 et 3.5 sont les mesures de S_{11} et S_{21} prises avec un analyseur de réseau.

3.3 - L'impact du synthétiseur multi-harmonique sur le système de load pull

La figure 3.6 est un exemple des impédances des trois éléments résonants à la fondamentale. La réflexion du deuxième et du troisième élément modifie l'impédance voulue par le synthétiseur fondamental. Donc le résonateur fondamental doit s'ajuster pour garder l'impédance stable pendant que les résonateurs harmoniques bougent. La même chose s'applique sur le troisième résonateur quand le deuxième résonateur bouge parce qu'il est placé devant celui-ci.

3.4 - La Calibration

Comme le synthétiseur fondamental, le synthétiseur multi-

harmonique est calibré en le branchant directement à l'analyseur de réseaux sous le contrôle du système hôte. Pour chaque position du deuxième résonateur le troisième résonateur est placé à dix positions différentes. Le deuxième résonateur est aussi placé à dix positions différentes. Ceci crée une matrice de 10X10. (15X15 et 20X20 sont maintenant aussi disponible.) Les paramètres-S sont mesurés à chaque position. Ce processus tient compte des effets de chaque résonateur sur l'autre. La calibration est faite à fo, 2fo et 3fo. Les données sont gardées dans un fichier de calibration et sont récupérés durant les mesures. Vû qu'il y avait trois fréquences fondamentales, il avait neuf matrices de 10X10.

3.5 - Le mouvement des résonateurs

La figure 3.7 compare le mouvement d'un résonateur le long de la ligne de transmission avec l'impédance sur l'abaque de Smith. La figure 3.8 montre les positions physiques initiales des deux résonateurs harmoniques et les impédances correspondantes.

3.6 - Les effets entres résonateurs

Les atténuations des résonateurs sont affectées par 1)leur position physique le long de la ligne de transmission 2)la fréquence à laquelle ils sont ajustés 3)les pertes dans la ligne de transmission 4) la distance entre les résonateurs.

La figure 3.9 montre comment l'impédance à la fondamentale varie durant un balayage de la deuxième harmonique. Vu que la longueur d'onde de la deuxième harmonique est la moitié de la fondamentale, son balayage sur l'abaque de Smith sera deux fois plus long. Le balayage de la troisième harmonique sera trois fois plus long.

Chapitre 4
Le montage et vérification du système de mesure

4.1 - Introduction

Les mesures ont été prises avec seulement un "through line" installé dans le fixture de test au lieu d'un transistor, dans le but de vérifier la calibration et la linéarité du montage et des instruments. Le montage est montré à la figure 4.1. La vérification a premièrement été faite avec les synthétiseurs fondamentaux installés, avant que le synthétiseur multi-harmonique ne soit installé à la sortie.

4.2 - Vérification utilisant un "through line"

Les étapes suivantes ont été suivies pour effectuer la vérification. Elles ont été suivies pour chaque fréquence fondamentale.

4.2.1 - Étape 1 - Vérification de l'impédance au plan du DST.

Si la calibration est bonne l'impédance sera au centre de l'abaque quand les synthétiseurs sont initialisés. Un $|\Gamma| < 0.05$ est considéré comme bon et acceptable.

4.2.2 - Étape 2 - Vérification du gain et linéarité

S'il n'y a pas de gain ou perte de G_T, Cela veux dire que les pertes du montage ont été bien prises en considération.

Quand la linéarité est bonne, ceci implique que le niveau minimum et maximum de la source et les atténuateurs placés devant les deux détecteurs de puissances sont bien ajustés pour le transistor en question.

4.2.3 - Étape 3 - Vérification de la calibration du synthétiseur fondamental

Un load pull complet avec le "through line", comme montré à la figure 4.3, montrerait s'il y a des irrégularités. C'est aussi la calibration de l'analyseur de réseau qui est vérifiée.

4.2.4 - Étape 4 - L'installation du synthétiseur multi-harmonique.

Les trois étapes précédentes ont été suivies pour ce synthétiseur. La figure 4.4 montre l'augmentation des amplitudes des coefficients de réflexions harmoniques après l'installation du tuner. Le $|\Gamma|$ de Z_L a aussi monté à peux près de 0.10 à 0.12 à cause des réflexions additionnelles non désirables du tuner multi-harmonique à la fréquence fondamentale.

4.3 - Vérification des deux synthétiseurs (fondamentale et multi-harmonique)

4.3.1 - Vérification de P_{OUT} pour les différent $|\Gamma_{Lfo}|$ durant les balayages harmonique (utilisant un transistor).

La figure 4.5 montre que les variations de puissance sont plus grandes avec une $|\Gamma_{Lfo}|$ plus grand. Les variations de plus que 2dBm pour le deuxième balayage harmonique et de près que 2dBm pour le troisième balayage, semblaient hors de la prédiction populaire

[4,5,7], avec un tel transistor (GHz, bipolaire, 0.5W, 2GHz) donc une raison pour garder $|\Gamma_{Lfo}| < 0.6$ a été constaté au début de ces études.

4.3.2 - Les variations de P_{OUT} durant les balayages de la deuxième harmonique pour les différents angles de la réflexion à la fondamentale, $\Delta\Gamma_{Lfo}$. (Utilisant un "through line", $|\Gamma_L| = 0.6$)

La figure 4.7 montre ces variations. La figure 4.6 montre les angles sur l'abaque ou les impédances sont plus stables. Les raisons et les théories sont donnés pour expliquer ce phénomène.

4.4 - Vérification de la stabilité des impédances fondamentale durant les balayages harmonique utilisant un analyseur de réseau

La figure 4.8 montre les deux synthétiseurs connectés ensembles et mesurés avec l'analyseur de réseau sous le contrôle du système hôte. L'impédance fondamentale était $\Gamma_L \approx 0.72\angle 180$. Les balayages harmoniques de 360° ont été effectués. Les résultats sont à la figure 4.9. Les figures montrent que l'impédance fondamentale (marker 1) est stable avec la fonction de correction activée est instable avec la fonction de correction désactivée. Les trajectoires sont désignées pour tous les balayages.

Comme expliqué, la trajectoire de l'impédance fondamentale est une demi-cercle pour un cercle complet de la deuxième harmonique et un tiers de cercle pour un balayages complet de la troisième harmonique.

Chapitre 5
Les mesures fondamentales du transistor

5.1 - Introduction

Le transistor de 3W a été installé et le synthétiseur multi-harmonique n'était pas installé. Le but des mesures était de trouver les meilleures impédances de source et de charge et le meilleur point de polarisation pour avoir le meilleur compromis entre la puissance et l'efficacité (PAE). Le signal de sortie ne devrait pas être trop distortionné et les terminaisons devraient être fabriquées sur micro-ruban. Ceci représente une situation réelle.

Les paramètres qui ont été variés durant les séances de load pull et de source pull étaient la fréquence, le point de polarisation, la compression, l'échantillon du même transistor et le but de performance (puissance ou éfficacité). Sept points de polarisation ont été mesurés comme montré à la table 5.1. Les tables 5.2 et 5.3 montrent les résultats pour des échantillons et impédances différents. Les résultats pour chaque point de polarisation sont présentés à l'appendice B.

5.2 - Les noms des fichiers des résultats

Les noms des fichiers représentaient les conditions de test. Un exemple est donné.

5.3 - Choisir le point de polarisation

Le graphique 5.1 montre les points de polarisation. À chaque point le load et source pull a été effectué sous des conditions

différentes.

5.4 - Les impédances Optimum

La relation entre la ligne de charge et l'impédance est expliquée. Pendant une séance de mesure de load pull, c'est l'optimisation de la pente et de la trajectoire de cette ellipse qui est cherchée.

5.5 - La méthode de tuning

Des fichiers de macro ont été utilisés pour assurer que les mêmes étapes ont été suivies à chaque fois. Ces mesures automatisées garantissent que les résultats seront répétables. Un exemple est donné et chaque étape est expliquée. Le tuning était manuel seulement pour trouver un compromis entre le maximum de puissance et d'efficacité. Trois types de fichiers de macro ont été utilisés pour trouver l'impédance idéale. Un pour compression, un pour non-compression, et une autre pour la réduction de "gamma".

5.6 - Les raisons pour diminuer Γ

Il avait des oscillations dû à l'instabilité du transistor et au système de mesure au bornes de l'abaque, donc l'amplitude du coefficient de réflexion a été diminuée à 0.6 pour choisir la meilleure performance. La diminution en performance était moins de 1dB est 3% en puissance et efficacité, respectivement. Une étude sur l'amélioration de performances d'un transistor dû aux terminaisons harmoniques peut être effectuée à n'importe quel point sur l'abaque, donc cette manoeuvre minime n'est pas grave à cette étude, qui a beaucoup à faire avec la mesure et le développement de ce synthétiseur harmonique et non seulement sur la performance maximale d'un FET.

5.7 - Les choix finaux de la polarisation et de l'impédance

Les choix finaux était Z_S=0.8/180°, Z_L=0.6/174°, I_D=200mA (16% I_{DSS}), V_D=8V. Les résultats finaux pour chaque fréquence sont donnés au tableau 5.4.

Chapitre 6
Les Résultats Comparatifs

6.1 - Introduction

Le synthétiseur multi-harmonique a été installé et l'optimisation à la deuxième et à la troisième impédance harmonique a été effectuée. Les résultats ont été comparés avec ceux sans l'optimisation harmonique.

6.2 - L'installation du synthétiseur multi-harmonique.

Après l'installation et l'initialisation du synthétiseur, l'impédance fondamentale à été aux mêmes valeurs qu'au chapitre 5 (tableau 5.4) et les mesures de performance ont été prises. Ceci est surtout pour avoir un bon point de départ auquel il est possible de retourné, si nécessaire, pour vérifier les conditions de test.

6.3 - L'optimisation multi-harmonique

L'optimisation à 1.8GHz et 1.85GHz était bonne. C'est à dire qu'il était possible d'avoir l'impédance fondamentale originale partout avec le nouveau synthétiseur en place. À 1.75GHz il n'était

pas possible d'obtenir l'impédance fondamentale originale à l'impédance harmonique optimisée. Ceci est causé par deux problèmes

1) Le synthétiseur multi-harmonique diminue le maximum de coefficient de réflexion à cause de sa perte d'insertion. Ceci est pire à 1.75GHz vue par le plus bas diamètre de points calibrés à la figure 6.1.

2) Le point d'impédance avec les deux synthétiseurs initialisés n'est pas rendu au centre de l'abaque. Donc il y a aussi des changements d'amplitudes, en plus des changements d'angle, quand il y a des changements de fréquence et des changements de positions des résonateurs harmoniques. Cette situation était pire à 1.75GHz.

6.4 - Comparaison des résultats

Le tableau 6.2 montre la comparaison des résultats entre l'optimisation avec seulement le synthétiseur fondamental et celle avec les deux synthétiseurs. Les comparaisons pour les autres fréquences sont à l'appendice C. La table 6.3 montre seulement les changements. Les résultats sont comparables à ce qu'il a été présenté [4,7]. Une seule déviation au tableau 6.2 est que l'amélioration en efficacité pour 2dB de compression devrait être plus haute qu'à 1dB de compression. Cette différence de -2% peut être due à l'incertitude du système.

Conclusion

Une impédance fondamentale et un point de polarisation ont été choisis pour satisfaire la stabilité de l'impédance fondamentale du système de mesure multi-harmonique et la performance d'un FET par rapport à la puissance et efficacité.

Après l'optimisation multi-harmonique l'amélioration était de 0.5dBm et 9% pour la puissance et l'efficacité, respectivement, et ceci pour une compression de 1dB.

Une fréquence au dessus et en dessous de la fréquence centrale a aussi été mesurée. À 1.85 les résultats étaient favorables, mais à 1.75GHz la perte d'insertion, et l'angle de la réflexion, causaient des problèmes de mesure.

Dû au fait que ce synthétiseur multi-harmonique vient d'être développé (le premier synthétiseur jamais construit a été utilisé pour cette étude) il était difficile d'attribuer les gains de performances à l'un ou l'autre des harmoniques. Dans les publications à date, ceci a rarement été fait avec succès avec un transistor de puissance, mais il sera possible de le faire bientôt, dû à la vitesse de développement chez Focus Microwaves. Il devrait être capable de le faire dans un environnement multi tonal.

Il sera possible de faire l'étude avec le synthétiseur multi harmonique toujours installé. Il a été enlevé du banc de mesure pour obtenir une plus haute amplitude de réflexion à la fondamentale.

Le transistor choisi devrait être monté dans un circuit micro-ruban. La conception de celui-là serai faite en accord avec les résultats de mesure du système multi-harmonique. Les mesures de

performances devraient être comparées avec ceux qui ont été prévues. Ceci validerait la "raison d'être" du système.

Table of Contents

List of Tables

List of Figures

List of Appendices

List of Abbreviations

Z_L or Z_{Lfo} - Total load impedance seen from the DUT reference plane at the fundamental frequency.

Γ_L - Total fundamental reflection coefficient seen from the DUT reference plane at the fundamental frequency.

Z_1 - Fundamental impedance component of a given part. (The contribution to the total fundamental impedance by a given part or portion of the setup.)

Γ_1 - Like Z_1, but concerning the reflected portion of the fundamental signal.

Z_2 or Γ_2 - Second harmonic impedance or reflection coefficient produced by a given part or portion of the setup.

Z_{L2fo} or Γ_{L2fo} - Load impedance or load reflection coefficient at the second harmonic.

Z_3 or Γ_3 - Third harmonic impedance or reflection coefficient produced by a given part or portion of the setup.

Z_{L3fo} or Γ_{L3fo} - Load impedance or load reflection coefficient at the third harmonic.

Z_s - Source impedance.

P_L - Power dissipated in the load.

P_{AVS} - Power available from the source.

P_{AVN} - Power available from the network.

P_{IN} - Power input to the network.

$|\Gamma_x|$ - Magnitude of the reflection coefficient.

$\angle\Gamma_x$ - Angle of the reflection coefficient.

Introduction

The ever increasing use of wireless communications has amplifier vendors searching for ways to make their products smaller, cheaper, more linear and more efficient; and to do this in the shortest design cycle time possible.

Since the late 80's the subject of providing optimized impedance terminations to the harmonic components generated by a device has gained an increasing amount of attention.

An advantage of harmonic optimisation is that a smaller, less expensive, transistor can be used in a given circuit, be driven into higher compression (area of higher non-linearity) to produce the same output power, signal to noise ratio, reliability, and be more efficient than its larger counterpart.

A disadvantage is that more "real estate" is taken up by the harmonic termination(s) in the final circuit layout, as well as more time being needed for design and test. But this disadvantage can be less significant than the extra cost of a larger microwave transistor which has a higher power need, or the lower performance of a non-harmonic optimised circuit.

Since most transistors are used in microstrip amplifiers with passive matching circuits, the passive impedance bench tuning topology more closely represents the conditions later obtained on microstrip. Most harmonic load pull systems require an active approach because power absorbing components, such as splitters and filters, are employed. The passive multi-harmonic tuner proposed in this work employs adjustable resonator probes, which act like microstrip "stubs", which absorb negligible power, and are placed between the device and the "fundamental" tuner.

This work is in collaboration with the Montreal based "Focus Microwaves" company which has produced such a passive multi-harmonic tuner (up to the third harmonic) to be used in their already established passive fundamental load and source pull systems. The first tuner of this type ever produced is used to perform harmonic load pull measurements on a 3W GaAs MESFET.

This study, with its encountered problems and successes are used for ideas and methods for improving the multi-harmonic load pull system. As much emphasis is therefore placed on the measuring and validating this harmonic load pull system as on the harmonic tuning of transistors themselves. Hopefully this study will contribute to another one in the near future which will use this system for the fundamental and harmonic load pull of devices only.

The first chapter discusses the general topic of load pull with some basic systems and configurations. The second chapter introduces the basic fundamental load pull system used. The system, the tuners, and their calibration is discussed.

The third chapter introduces the multi-harmonic tuner and its basic operation and impact on the system. Some of the details and nuances of the multi-harmonic tuner and system are studied and presented. The tuner is validated on a network analyser and in a load pull system containing only a through line. (A through line does not produce any harmonics and therefore harmonic tuning should not show any variations at the output.)

In the fourth chapter the general fundamental load pull set up is verified in a step by step manner which can apply to other systems as well. Then the multi-harmonic tuner is installed and specific verification and validation processes are undertaken using a network analyser, a through line and a transistor.

In Chapter 5 the multi-harmonic tuner has been removed and the 3W MESFET is installed. Official fundamental load and source pull measurements are undertaken as the final bias, load and source impedances are chosen. This sets up the conditions under which harmonic impedance optimisation will take place.

In Chapter 6 harmonic load pulling is performed and the performance results (and improvements) are compared with those of Chapter 5. The results are tabulated and discussed. Then, a conclusion is drawn for the entire work.

CHAPTER 1

Fundamental and Harmonic Load Pull Systems

1.1 - Fundamental Load Pull

Load pull is a measurement technique whereby an output parameter of a device is measured (typically power) as its load impedance is changed, giving the "output power/load impedance" relationship sought. The load impedance is modified using an adjustable tuner. Part of the signal generated by the device is returned with modified amplitude and phase which interacts with the signal leaving the device, thus modifying its operation.

Using computer simulations is the preferred method of design nowadays, as compared to bench measurement setups, due to their ease of operation and design speed. However, this "wave interaction" is difficult to computer simulate in nonlinear situations, so practical load pull bench setups are widely in use today. Bench setups are especially important for analysing the output of transistors operating in large signal (nonlinear) mode where harmonics are generated. The measurement results are used for amplifier design, computer model verification, and for verifying specifications given in manufacturers' data sheets. Manufacturers usually offer little, if any, information on this important (load pull) topic [10] leaving amplifier vendors in the dark even if computer simulations were more accurate.

"Source pull" can also be performed whereby an output parameter is measured as the source impedance is changed by a tuner connected at the input.

A classic load pull set up is shown in Fig 1.1.

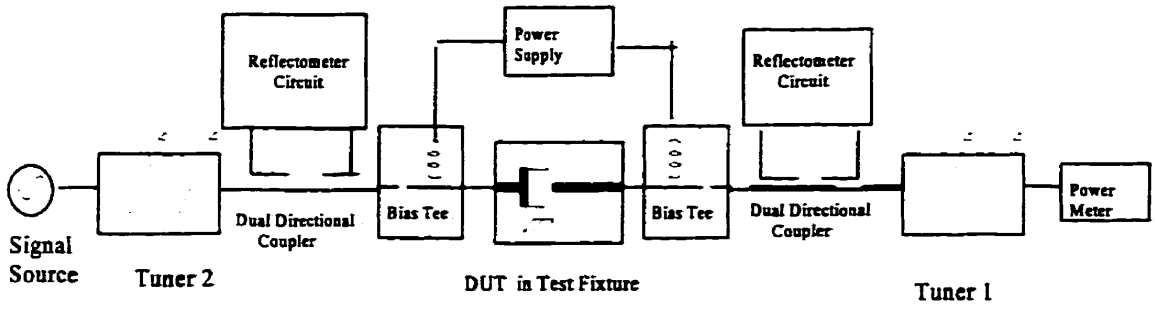


Figure 1.1 - Classic Passive Load Pull Set Up

The dual directional couplers are used as reflectometers to measure the reflection coefficients of the input and output tuners so that the power into and out of the device can be determined. One thus obtains the gain and output power of the device corresponding to various tuner loads. From this the power and gain contours can be drawn. Six-Port reflectometer techniques [3] can be used which would be partly represented by the "Reflectometer Circuit" block.

Without the dual directional couplers, Z_L and Z_s can be obtained by removing the manual tuners from the setup and measuring them on a slotted line or a network analyser. It should be mentioned that tuners of this type are passive, and therefore linear, their impedance will not change with the different signal power of a network analyser. Removing and inserting tuners is a cumbersome operation which can lead to measurement inconsistencies, so using dual directional couplers, or a method of "in circuit" measurement, is more convenient and accurate.

The following signal flow graph and equations define some of the reflections and gains derived from power measurements.

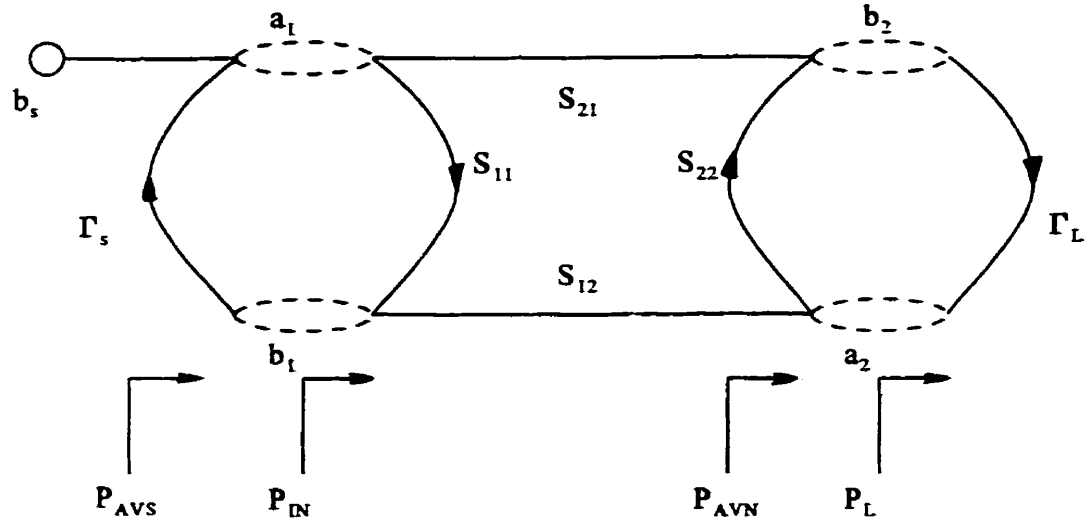


Figure 1.2 - Reflection and Power Definitions

Transducer gain: $$G_T = \frac{P_L}{P_{AVS}} \qquad (1.1)$$

Available gain: $$G_A = \frac{P_{AVN}}{P_{AVS}} \qquad (1.2)$$

Operational Gain: $$G_P = \frac{P_L}{P_{IN}} \qquad (1.3)$$

A setup which does not rely on dual directional couplers, per se, (although there are surely some employed within the measurement instruments shown) and in which the tuner does not need to be removed, is shown in Figure 1.3 [2].

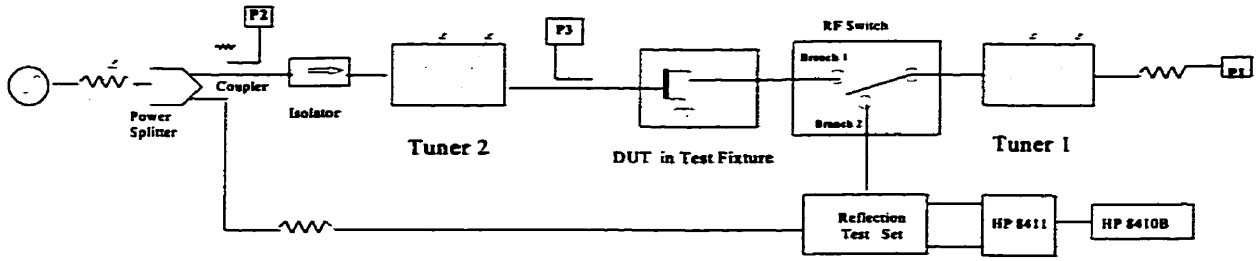


Figure 1.3 - Load and Source Pull Set-up without Reflectometers

At a given frequency, transistor bias, and input power (measured on P2), the input tuner is adjusted for optimum return loss, as measured on P3 (typically 25 dB return loss can be attained[2]). This is done by adjusting Tuner 2 to have the lowest possible reading of power on P3. In this way P2, which represents P_{AVS}, will likewise represent P_{IN}, since the input is adapted. There is a negligible amount of reflected power from the input and therefore it is considered that the transducer gain, G_T, equals the operating gain, G_p, since $P_{AVS} = P_{IN}$. G_T is what is actually measured from the power readings of P1 and P2.

With the SPDT (Single Pole Double Throw) switch connected to branch 1, Tuner 1 is tuned for the output gain and power desired. By switching the SPDT to branch 2, the output impedance provided by this output tuner can be read directly if the electrical lengths of the two branches are identical. Thus, the output load impedance which gives the desired performance can be obtained directly (for a given bias and frequency).

The input tuner's impedance cannot be measured while in the circuit. This is usually not a problem since load pull measurements are used to study behaviour at the output of a device and not at the input. Note that when performing noise measurements, for instance,

where non-adapted source impedances need to be studied, a setup with a means of knowing this source impedance, such as with the dual directional coupler, or a similar setup as shown above for the input, is required.

1.2 - Active Load Pull

In this approach a "virtual load" is presented to the output of the DUT by injecting into it a signal synchronized with the measured signal instead of by reflecting it off a passive load (tuner).

There are two ways of generating this injected signal:

1. Takayama Method [28]: The input signal is split before the DUT and has its amplitude and phase modified before it is injected into the output via the bypass branch. See Figure 1.4.

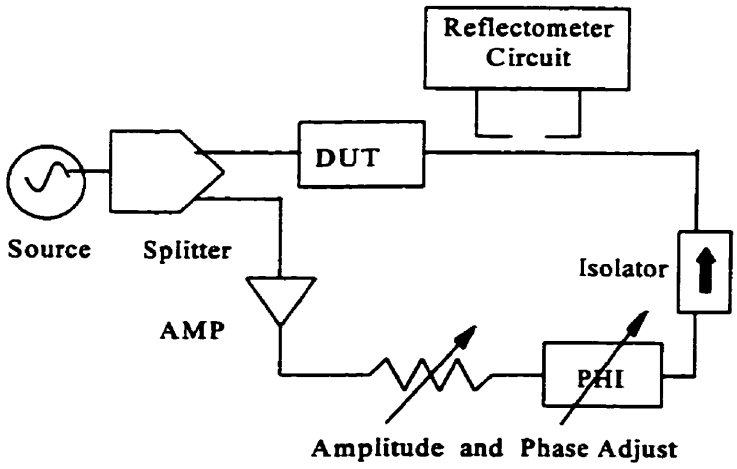


Figure 1.4 - Takayama Method

2. Active One Port Load Method. The signal is split after the DUT and its amplitude and phase is modified before it is reinjected back into the output. See Figure 1.5.

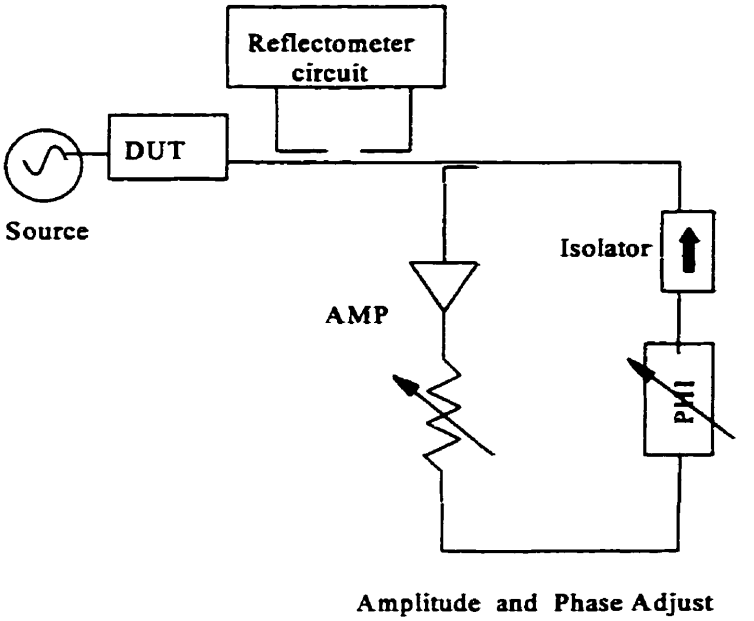


Figure 1.5 - Active One Port Load Method

The advantage of an active approach is the increased range of load impedances available compared to a passive approach. The entire $\Gamma=1$ Smith chart can be covered (and more) whereas in a passive setup the range is limited due to insertion losses of the test fixture, tuners and other components. A reflected wave of greater than 0.85 of the incident, at the DUT reference plane, is considered good. An active setup will have the amplification to overcome any losses. There is no phase limitation in either system. Albeit their added complexity, active systems are more versatile if control is often required at reflection factors of 0.85 and higher.

1.3 - Harmonic Load Pull

Since the late 80's the subject of providing optimized impedance terminations to the harmonic components generated by a device has gained an increasing amount of attention.

Performance gains through harmonic optimization become more significant as the transistor is made to operate with a larger signal, or in a more nonlinear region, or with a higher level of saturation or compression. (These last terms all have the same meaning.) These increased harmonics appear at "hfo" where h=2,3,4...∞, and fo is the fundamental frequency which appears at the input of the device.

The goal is to recover some of the energy which would normally be lost in the harmonics, and to "recycle" it in order to a) increase the fundamental component, thus increasing the output power and b) reduce the DC energy required to produce this RF energy, thus increasing the efficiency. It is generally agreed that the efficiency gains are greater than the power gains.

Power gains due to second harmonic terminations have been reported from 0.4dB [4] to 1.5dB [7] and power added efficiency (PAE) gains from 4.1% [4] to 12% [7].

Power Added Efficiency (PAE) gains of the third harmonic have been reported as "weak" [5], "contributes to refining the potential high efficiency behaviour" [10], to 10%[11].

To the knowledge of the author, it is unanimously agreed upon that the fourth and higher order harmonics contain insignificant energy to warrant much effort in tuning for them.

In order to recover energy from a harmonic, it is necessary

that as much of it as possible is reflected back to the device where it can be "recycled". The higher the magnitude of the reflection coefficient at the harmonic frequency, the more potential there is for a performance enhancement at the fundamental and DC level. Total reflection implies that the device sees either a short or open circuit.

"Third harmonic peaking class-F" amplifiers have been suggested for microwave amplifiers [13] in the late 1980's. Here a power match is provided at the first harmonic (fundamental) a short circuit is presented at the second harmonic and an open circuit at the third harmonic. More accurate optimizations of the terminating impedances have since been studied.

The increase in efficiency results from reduced power dissipation. Controlling the harmonics is in essence wave shaping the voltage and current waveforms at the device to reduce the power dissipated in it [13].

The single most important fact in harmonic tuning is that it is the phase of a highly reflected harmonic that needs to be optimized. This is where the commonly used expression "phase of the short circuit" comes from, even though the load can be an open circuit or an active circuit.

At high magnitudes of harmonic reflection coefficients, $|\Gamma_{Lhfo}|$ (h=2,3), it becomes important to optimise the phase angle, $\angle\Gamma_{Lhfo}$ (h=2,3), since device performance can decrease as well as increase [4] relative to a non-reflective termination (50Ω). Harmonic phase optimization when $|\Gamma_{Lhfo}|$ is low is less important since most of the harmonic energy is absorbed by the circuit or load before it can be recycled upon returning to the device. It is important to remember that even a load which has been optimized for only the fundamental signal also presents a certain impedance to the harmonics, and may

be part of the reason why that "fundamental" load was chosen in the first place. "True" fundamental load pull implies that signals at other frequencies see 50Ω (or a given setup's characteristic impedance). However with some "fundamental" setups the operator is "unaware" of the harmonics. Harmonic load pull techniques attempt to firstly diminish the effects of the "fundamental" load on the harmonic signals so that independent control can be gained. Then the second and third harmonic loads must also be made independent of each other. The fundamental load, Z_{Lfo} (or sometimes labelled Z_L in this report) should affect only the fundamental signal f_o, and the second harmonic load Z_{L2fo} (or sometimes labelled Z_2 in this report) should affect only the second harmonic $2f_o$, and so on.

This is easier to do in a computer simulator than in practice. Many load pull setups use splitters and filters to separate and process the signals. This requires an active approach in order to overcome the losses created by these components. In a passive approach, power absorbing devices are prohibitive because the reflection coefficient will become too low to make a significant performance change. A novel, and inexpensive, method for microstrip is to place open circuit stubs directly on the output half of the test fixture as shown in Figure 1.6.

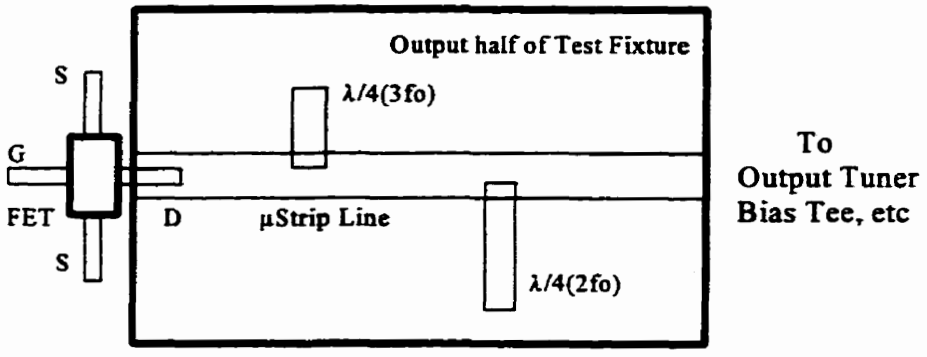


Figure 1.6 - A Novel Microstrip Multi-Harmonic Tuning Method

Foil of a length calculated to be a quarter wavelength of a given harmonic can be "slid" along until the performance is optimized. Open circuited stubs of one quarter wavelength present a short circuit at their opposite ends. Thus, sliding it along (or more likely taping it from one location to the next) in a half wavelength distance (which is once around the Smith chart) varies "the phase of the short circuit". Since the stubs present no real part to the signal (losses), the reflection coefficient at the fundamental is not reduced and full tuning capability of the fundamental tuner is conserved [9]. Furthermore, since the stubs are close to the DUT, the needed high reflection coefficients at the harmonics do result. Also, since there aren't any harmonics reaching the fundamental tuner, because they are being reflected back to the device, it is no longer a problem if the "fundamental" load is not "narrowband".

Still another advantage is that this is a realistic final microstrip topology, so big differences should be less probable when going from the measurement setup to the final design. If the stubs

do present some reflection to the fundamental component, they will more or less do so in the final microstrip design. In order to achieve the specified performance for any device, the design of the amplifier should closely resemble the test circuit [10].

A definite disadvantage of this method is the inconvenience of moving stubs using tape or some other way. It is not repeatable or reliable because it is ad hoc and messy. It is a prototype affair and not a "Test Engineering" solution. However, the advantage of this topology suggests some merit for a passive load pull solution.

CHAPTER 2

The Proposed Automated Passive Load Pull System

2.1 - Introduction

The load pull system used in this work was developed by the "Focus Microwaves" company located in the Montreal area. The computer controlled microwave tuner (CCMT) has relatively low insertion loss, offering reflection factors of up to 0.98 at the tuner reference plane. Once the setup has been calibrated using the host system's software and a network analyser, the system "knows" the impedance seen from various reference plans, such as from the input and output of the transistor under test. The major advantage of this is that the setup does not need to be broken up in order to measure the tuners' impedance values, and the network analyser (typically any lab's most expensive and demanded piece of equipment) does not need to be used again and is freed up for other tasks. The system's computer screen shows a Smith chart with the source and load impedances displayed "live" on the screen as the tuners' impedance is changed via keyboard or mouse control. Measurements, such as power, gain, DC bias and efficiency, can also be displayed on the screen upon operator request using the integrated GPIB measurement system.

The basic fundamental load pull system will first be discussed before introducing the "add-on" passive harmonic tuning device in Chapter 3 which allows harmonic load pulling as well.

The fundamental load pull setup is shown in figure 2.1.

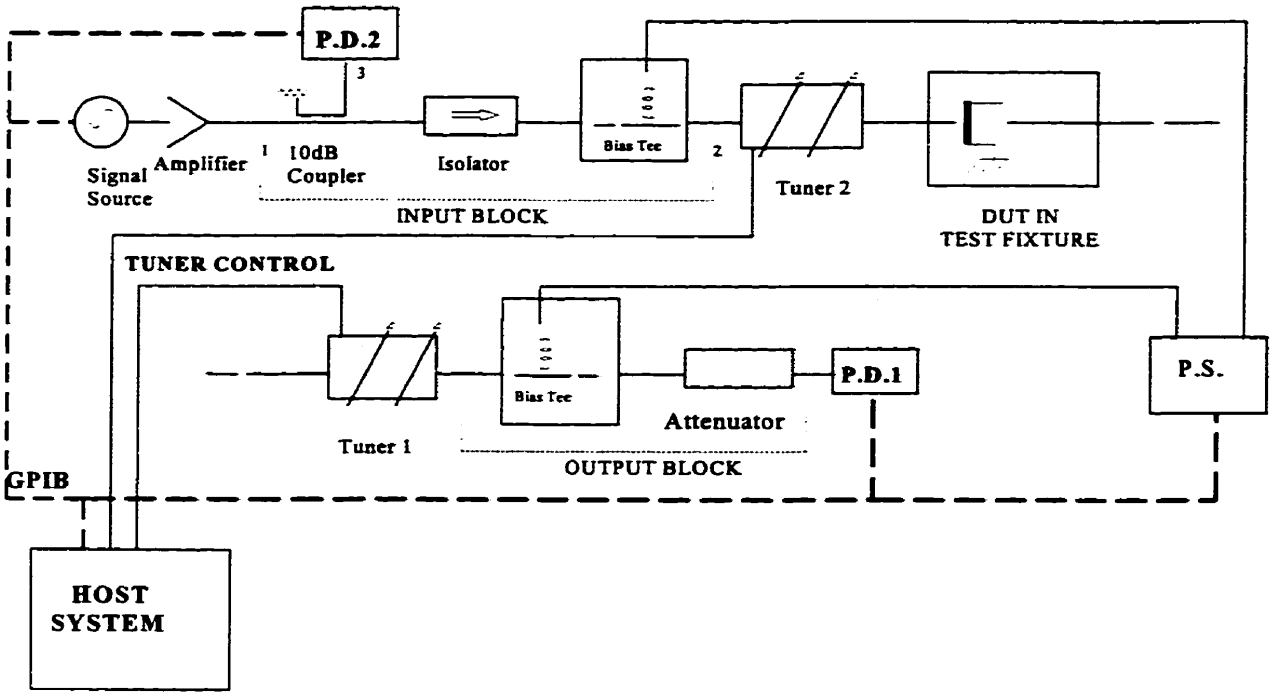


Figure 2.1 - Fundamental Load Pull Set Up

The system differs from that of Figure 1.3 in that it uses only two power meters. Optimum return loss is found by tuning the input until maximum gain is found at the output, not until minimum power is found on "P3" of Figure 1.3. Then $P_{avs} = P_{in}$. The advantage of this is that only one dual channel power meter is required. A coupler and power meter could be added if one is needed to measure the return loss.

2.2 - The Automated Programmable Tuners

The microwave tuners designed and manufactured by "Focus Microwaves" are electro-mechanical devices based on a probe moving along a precisely slotted coaxal airline. Two high-resolution stepper motors ensure exact mechanical positioning of the probe in two directions- up and down, (in and out) of the airline to provide the desired attenuation, and lengthwise along the airline to control

the phase of the load.

As is intuitive, the more into the airline the probe protrudes, the greater will be the attenuation (or reflection) of the signal. This is the real value of the impedance. And as the probe moves in the "x" direction along the transmission line, the phase at which the wave will be attenuated is varied. This is the imaginary part of the impedance.

The probe is designed to provide repeatability and vibration insensitivity [21]. The size of the insertable slug limits the obtainable VSWR. The length of the slotted airline limits the obtainable phase control ($\lambda/2 = 360°$ in reflection).

Many of these factors apply also to manual screw type tuners. The motors, motor control circuitry and interface, allow the tuning operation to be controlled by the host system.

2.3 - Calibration

Every component in the system must be calibrated in order to be able to shift reference planes and calculate losses. Before components can be calibrated the network analyser must first be accurately calibrated, especially when dealing with the high reflection coefficients of the tuners [12]. The HP8753D Network Analyser was calibrated using a TRL method using standards produced and marketed by "Focus Microwaves". TRL calibration is covered in the Test Fixture Calibration section.

All components must be calibrated at the same frequency in order to be able to shift reference planes. This is because the S-parameters will be different at different frequencies, prohibiting the cascading of S-parameters.

2.3.1 - Tuner Calibration

The fundamental tuner is first calibrated using a Network Analyser. It is calibrated at up to 361 combinations of the resonator's x and y positions. The CCMT system reads and records the S-parameters (two port S-parameters) of the unit at each tuner position. This S-parameter matrix is composed of eight numbers- four magnitudes and four angles. The tuner calibration file will therefore contain 361 lines of 8 numbers each. Once in operation, the S- parameters of the tuner is known for each position of the resonator probe, or they can be extrapolated, given the even spread of calibrated points on the impedance plane.

2.3.2 - Setup Calibration

The S-parameters of the input block, test fixture and output block are placed into another calibration file- the "setup calibration file". For each frequency, this file contains a set of S-parameters for each block. Since a set of S-parameters is eight numbers and there are as few as four blocks, this file can contain a minimum of one 3X8 matrix, if only one frequency is calibrated.

2.3.2.1 - Input block

Aside from the four S-parameters representing the transfer between port 1 and 2, the coupling factor between port 1 and 3 must also be included in the file to enable the input power measurements. For the coupling, only one S-parameter magnitude- $|S_{31}|$, is recorded. The angle of S_{31} is not required because a power reading is taken at port 3, which is not phase sensitive.

2.3.2.2 - Test Fixture Calibration: The TRL method

The test fixture is calibrated on the Network Analyser using the TRL method under host system control.

This network analyser technique is needed to be able to "know" where the DUT is in the test fixture. It effectively measures the transmission lines of the test fixture so that their effects can be removed, enabling the representation of the measurements at the DUT reference plane. This is known as "de-embedding". Many network analysers are calibrated using the TRL method. The three TRL standards are "Through", "Reflect" and "Line".

Through: The two test fixture halves are screwed together, creating a "through line" of 50Ω. A one inch (approx) strip of gold leaf, having the same width (or slightly less) as the microstrip, is taped across the gap to make the through line continuous. The total length of the two halves of the test fixture must be equal to the total length of the THROUGH, i.e. nothing can be inserted between the two halves when the measurement is taken.

Reflect: The gold leaf strip is removed and the two test fixture halves are unscrewed and moved away from each other. The gap between the two halves must be at least two inches, ensuring that the wave on each half is reflected during the measurement by the open circuit created by this large gap.

Line: A delay line having a known characteristic impedance (usually 50Ω) is inserted into test fixture between the two halves and the three elements are screwed together. Gold leaf strip (usually the same one) is taped across the delay and the two small gaps to ensure continuity. The length of the delay line should be near a quarter of the transmission wavelength at the centre frequency to give good precision and operating bandwidth.

Theoretically the line must be less than 180° longer than the minimum intended wavelength. With a good calibration it is possible to yield fmax/fmin ratios beyond 36:1 using a single delay line [12]. For the third harmonic measurements used in this work, including a 5% bandwidth, a ratio only slightly higher than 3:1 is required- so the delay line length is not critical here.

2.3.2.3 - Output Block

This block is calibrated like the input block, without the S_{13} measurement. Up to 30dB of attenuation can be calibrated directly on the network analyser, after this the extra attenuation needs to be written into an "attenuation" file. This is due to a C programming arithmetic limitation.

2.4 - Shifting Reference Planes

In order to know the load impedance, Z_L, seen from the DUT reference plane, it is necessary to know Γ_L (S_{11}) seen from this plane (and the characteristic impedance, Z_o). After calibration, the S-parameters of the tuner and subsequent components is known. S_{11} must be found looking from the output of the DUT so that the load impedance can be found.

Finding S_{11} at the DUT reference plane is done by cascading the S-parameters of the output half of the test fixture, the output tuner, and the output block. The tuner will of course have the biggest contribution. When cascading these networks, "chain scattering parameters" or "T parameters" are used in which the dependant variables are the input waves, a_1 and b_1, and the output waves a_2 and b_2 are independent. This makes cascading convenient because, as seen in Figure 2.2, the output waves of one block are equal to the input waves of the next block.

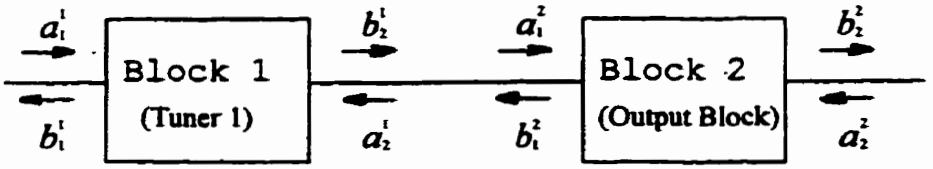


Figure 2.2 - Cascading Blocks

block 1:

$$\begin{bmatrix} a_1^1 \\ b_1^1 \end{bmatrix} = \begin{bmatrix} T_{11}^1 & T_{12}^1 \\ T_{21}^1 & T_{22}^1 \end{bmatrix} \begin{bmatrix} a_2^1 \\ b_2^1 \end{bmatrix} \qquad (2.1)$$

block 2:

$$\begin{bmatrix} a_1^2 \\ b_1^2 \end{bmatrix} = \begin{bmatrix} T_{11}^2 & T_{12}^2 \\ T_{21}^2 & T_{22}^2 \end{bmatrix} \begin{bmatrix} a_2^2 \\ b_2^2 \end{bmatrix} \qquad (2.2)$$

Since the waves at the output of block 1 are equal to the input of block 2:

$$\begin{bmatrix} a_2^1 \\ b_2^1 \end{bmatrix} = \begin{bmatrix} a_1^2 \\ b_1^2 \end{bmatrix} \qquad (2.3)$$

And therefore:

$$\begin{bmatrix} a_1^1 \\ b_1^1 \end{bmatrix} = \begin{bmatrix} T_{11}^1 & T_{12}^1 \\ T_{21}^1 & T_{22}^1 \end{bmatrix} \begin{bmatrix} T_{11}^2 & T_{12}^2 \\ T_{21}^2 & T_{22}^2 \end{bmatrix} \begin{bmatrix} a_2^2 \\ b_2^2 \end{bmatrix} \qquad (2.4)$$

Which gives the relationship across two blocks. The relationship between S and T parameters are:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{T_{21}}{T_{11}} & T_{22} - \frac{T_{21}T_{12}}{T_{11}} \\ \frac{1}{T_{11}} & -\frac{T_{12}}{T_{11}} \end{bmatrix} \qquad (2.5)$$

and

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{S_{21}} & -\frac{S_{22}}{S_{21}} \\ \frac{S_{11}}{S_{21}} & S_{12} - \frac{S_{11}S_{22}}{S_{21}} \end{bmatrix} \qquad (2.6)$$

Once S_{11} seen from the DUT is found, the system can calculate the impedance seen from the device from the basic Smith chart formula:

$$Z_L = Z_o \frac{1+\Gamma_L}{1-\Gamma_L} \qquad (2.7)$$

where $\Gamma_L = S_{11}$ seen from the DUT reference.

Using the same procedure, the DUT's source impedance Z_s can be found by cascading the S-parameters of the input tuner and the input block. This procedure is general and is actually more useful when more than two blocks are being cascaded. When there are only two blocks, the equation 3.1 can also be applied.

2.5 - Power Measurements and Calculations

The power at the DUT output can be calculated by adding from the P.D.1 reading the losses of all the blocks between the DUT and the power detector head:

$$P_{OUT} = PD_1 + L_{Att} + L_{B.Tee} + L_{T1} + L_{O/P\_Fixt} \quad (2.8)$$

Where L are the power losses given by:

$$L = \frac{1-|S_{11}|^2}{|S_{21}|^2} \quad (2.9)$$

The power at the DUT input can be calculated by first adding to the PD2 reading the losses of S_{13}, which is the coupling factor, and then subtracting the losses of the input blocks:

$$P_{IN} = PD_2 + L_{13} - L_{B.Tee+Iso} - L_{T2} - L_{I/P\_Fixt} \quad (2.10)$$

CHAPTER 3

The Multi-Harmonic Tuner and Multi-Harmonic Load Pull System

3.1 - Introduction

The Multi-harmonic tuner (or the Programmable Harmonic Tuner, PHT, as it is officially referred to by the Focus Microwaves company) is installed in the system before the "fundamental" tuner and after the DUT as shown in Figure 3.1. The second harmonic signal is reflected by the "2fo stub resonator" and the third harmonic by the "3fo stub resonator". The dimensions of these resonator probes are manufactured in accordance to the desired frequency of operation.

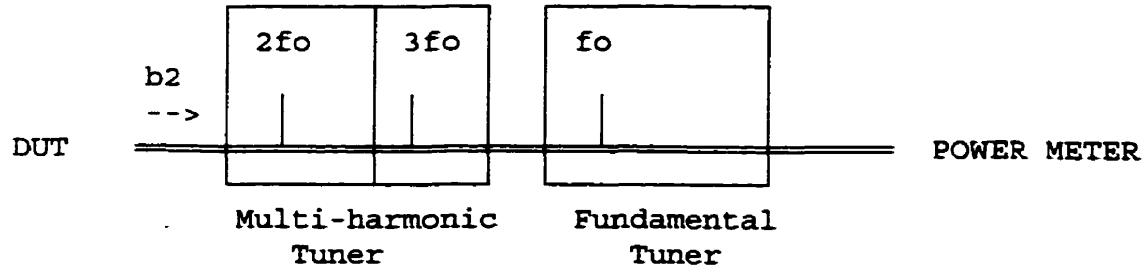


Figure 3.1 - Serial layout of the frequency elements

The topology of the resonators in these tuners is similar to that of the microstrip harmonic tuning example presented in Figure 1.5.

The fundamental impedance is synthesised by the load tuner as before. Ideally, due to this "serial" topology, the fundamental tuner will not have an effect on the harmonics because they have already been reflected back to the DUT by the preceding elements.

The same applies to the 3fo probe as far as second harmonics are concerned. It is important that the 2fo resonator doesn't present a significant reflection to the first (fundamental) and third harmonics in order to maintain this independent control. This can be shown by the following reflection coefficient formula:

$$\Gamma_{Lhfo} = S_{11A} + \frac{S_{12A}S_{21A}\Gamma_B}{1 - S_{22A}\Gamma_B} \quad (3.1)$$

Where Γ_{Lhfo} is the total load reflection coefficient at a given harmonic looking from the DUT reference plane and all involved S-parameters are those of the given harmonic as well. "A" refers to the Multi-harmonic tuner shown in Figure 3.1 and "B" refers to the fundamental tuner.

Because the fundamental tuner is followed by a 50Ω bias Tee component and a power detector which offer a negligible amount of reflection, it can be assumed that:

$$\Gamma_B = S_{11B} \quad (3.2)$$

Therefore the formula becomes:

$$\Gamma_{Lhfo} = S_{11A} + \frac{S_{12A}S_{21A}S_{11B}}{1 - S_{22A}S_{11B}} \quad (3.3)$$

In the case of the first harmonic, it can be seen that S_{11A} and S_{22A} must be small (forward and reverse reflection of the Multi-harmonic tuner) and that S_{12A} and S_{21A} (forward and reverse transmission of the Multi-harmonic tuner) must be large in order for the fundamental tuner, which controls S_{11B}, to have the greatest influence.

In the case of the second harmonic, the opposite is true, in order that the Multi-harmonic tuner has the greatest influence (S_{11A})

and that the fundamental tuner (S_{11B}) has the least influence on the second (and third) harmonic.

The expression can also be used to study the effect of the second harmonic resonator on the third and vice versa.

3.2 - Multi-Harmonic Tuner Movement

The harmonic resonator probes move along the x axis within their "enclosures" which are long enough to cover a half wavelength at the harmonic frequency. This allows the phases of the harmonic impedances to move completely around the Smith chart. The reflection coefficient is always high due to the nature of a stub.

This set up thus allows load pull tuning of the first (the fundamental), second, and third harmonic. Such a multi-harmonic tuner can also be installed between the source tuner and the device in order to perform harmonic source pull tuning as well.

The dimensions of the resonant probes tunes them to their desired harmonic frequency. Having these manufactured to fixed dimensions is generally not a disadvantage since most users perform their measurements within the same band. Stub resonators typically have a bandwidth in the order of 10%, as is the case here. The centre frequencies are screw adjustable by about ±10%. For this work the fundamental frequency band was from 1.75 to 1.85GHz (5.5% bandwidth), the second harmonic was therefore 3.5 to 3.7GHz and the third harmonic 5.25 to 5.55GHz. No screw adjustment was actually ever needed.

The harmonic tuners' attainable impedance looking into the multi-harmonic tuner from the test fixture output half for the second and third harmonic- 3.6GHz and 5.4GHz, are shown in Figure

3.2 and 3.3. This shows the level of reflection magnitude. As can be seen in Appendix A1, the reflection factors of the harmonics of 1.75GHz and 1.85GHz are still very high. The synthesised impedance can also be placed in-between these indicated points since the resolution of the motors is higher than that shown. When positioned in between calibrated points, the software extrapolates the S-parameters. The third harmonic tuner has a slightly lower magnitude of reflection because of the slightly higher losses associated with being a greater distance away from the DUT reference plane.

Figure 3.4 shows the transmission characteristics of the multi-harmonic tuner measured on the network analyser. As expected, the forward transmission at the second and third harmonics (3.6 and 5.4 GHz) is very low because they are reflected by the stub resonators. The signals in the vicinity of 1.8GHz is high as these signals will pass on to the fundamental tuner.

Figure 3.5 shows the forward reflection coefficient of the multi-harmonic tuner. In the 1.8GHz area the reflection is low and in the 3.6GHz and 5.4GHz area it is high. It can be suggested that an improvement in the return loss (lower reflection) can be beneficial at 1.8GHz.

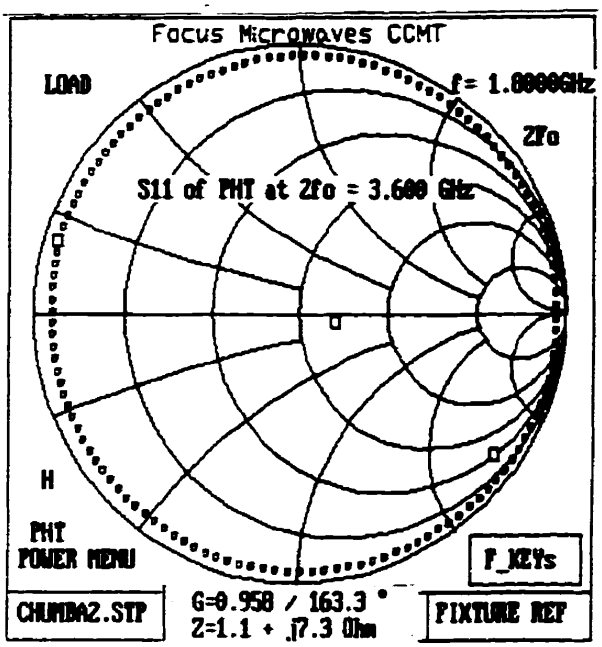


Figure 3.2 - Second Harmonic Impedance Points

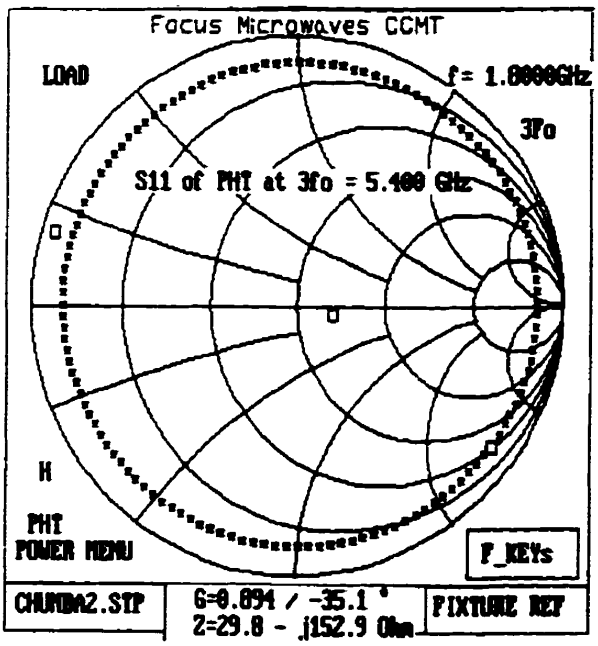


Figure 3.3 - Third Harmonic Impedance Points

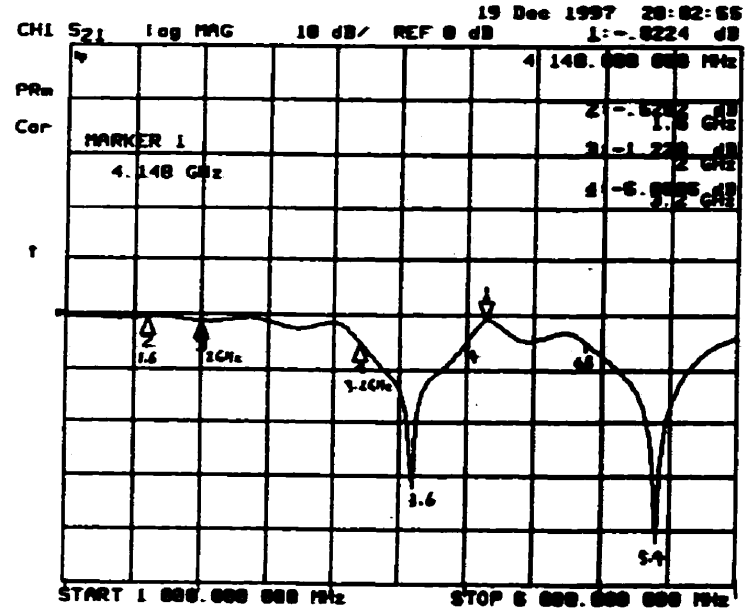


Figure 3.4 - Forward Transmission of the Multi-Harmonic Tuner

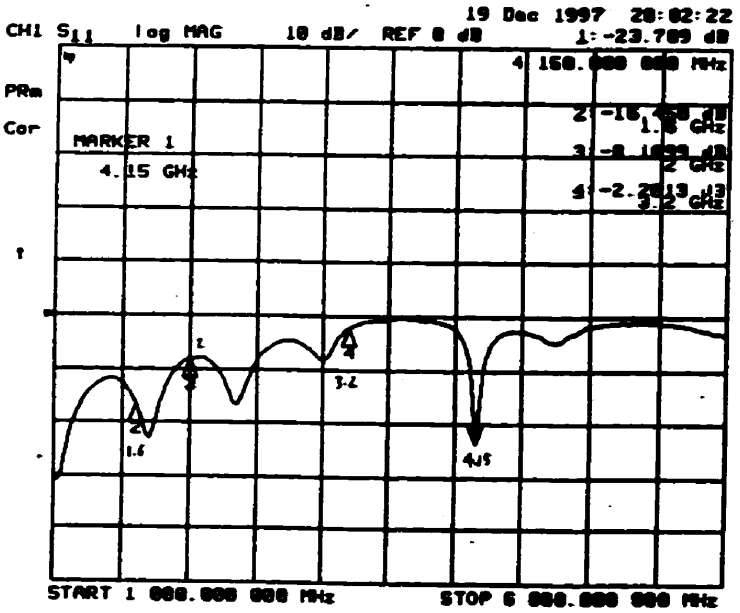


Figure 3.5 - Forward Reflection of the Multi-harmonic Tuner

3.3 - Impact of the Multi-Harmonic Tuner on the Load Pull System

Placing the harmonic tuner between the DUT and the fundamental tuner does increase slightly the insertion losses between the DUT and fundamental tuner and reduces slightly the maximum reflection attainable at the fundamental. This can affect lower impedance devices (power devices) more since larger devices require that the network losses be lower due to their generally lower output impedances [5]. However this can be accounted for if needed by using quarter wave impedance transformers, which will be discussed later.

Figure 3.6 shows the impedance of all three elements at the fundamental frequency. The "first" element is the "fo" resonator of the fundamental tuner acting on the fundamental signal (1.8GHz). In this example it is tuned to give a reflection magnitude $|\Gamma_L|$ of approximately 0.8. The "second" element, the 2fo resonator, presents a small impedance to the fundamental signal due to its non-ideal response. The "third" element, the 3fo resonator, presents an even smaller magnitude of reflection since it is tuned to a more distant frequency.

The total impedance is the vector sum of all three vectors. The system software calculates this result by cascading the three sets of S-parameters and calculating Z_L from the resulting S11.

A system problem which needs to be overcome when the harmonic elements are placed ahead of the fundamental one is in keeping the total fundamental impedance constant and at the intended value as the harmonic elements are tuned. The system must calculate the total impedance each time a harmonic resonator is tuned and then

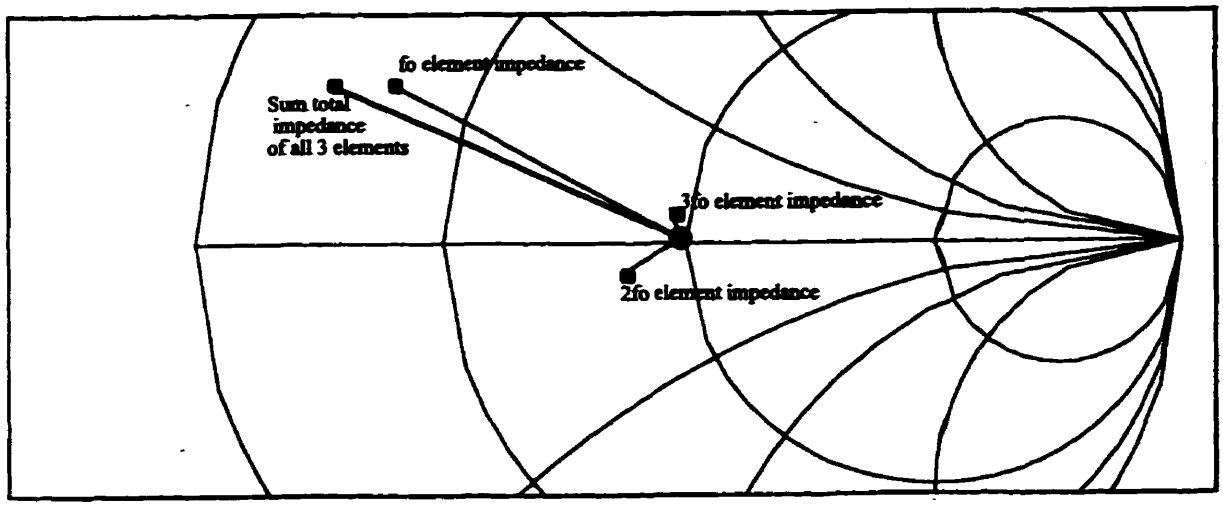


Figure 3.6 - Impedance of each Element at 1.8GHz

adjust the fundamental tuner, if necessary, to hold the total fundamental impedance fixed. The same applies to adjusting the third harmonic impedance when the 2fo resonant probe is moved, since it is in front of this impedance element.

3.4 - Calibration

Like the fundamental tuner, the multi-harmonic tuner is calibrated on the network analyser under system control through the GPIB bus. For each position of the 2fo resonator, the 3fo resonator is moved to 10 evenly spaced positions (15 and 20 positions are now also available). The S-parameters are recorded at each of these positions. The 2fo resonator is positioned to 10 evenly spaced positions, creating a 10X10 matrix of two port S- parameter for each frequency. For a given fundamental, fo, the tuner will also be calibrated for the two harmonics, 2fo and 3fo, so there are 3 sets of 10X10 matrices for each s parameter for each fundamental. In this work three fundamentals were used: 1.75, 1.80 and 1.85GHz, so the device was calibrated at nine frequencies at 100 physical tuner

positions each, resulting in 900 two port S-parameters. This data is stored in a Multi-harmonic tuner calibration file to be recalled each time the tuner is re-positioned or if the frequency of interest is changed.

This procedure will characterise the entire Multi-harmonic tuner and take into account the effect of both resonators at a given frequency for a wide combination of positions. During measurement, the S-parameters which are later recalled from the calibration file are the ones recorded for the current tuner position and frequency. If an in-between position has been tuned to then an extrapolation will take place between the two closest S-parameter sets. There is no extrapolation between frequencies.

3.5 - Resonant Probe Movement

The resonant probes are open circuited stubs one quarter wavelength of the harmonic long, therefore presenting a short circuit to the harmonic at the end which is connected to the co-axial air (transmission) line.

Fig 3.7 compares the resonant probe movement along the airline with that of the impedance on the Smith chart. The impedance on the Smith chart represented by a given position on the airline depends on the resonant probe's distance in wavelengths from the DUT. The reflection coefficient is always high since it is a stub. It is the "phase of the short circuit" that is changing. As the stub leaves the right hand side (RHS) position and moves towards the device the phase moves counter clockwise (a positive change in degrees). This is comparable to "removing" some of the transmission line between the stub and the DUT.

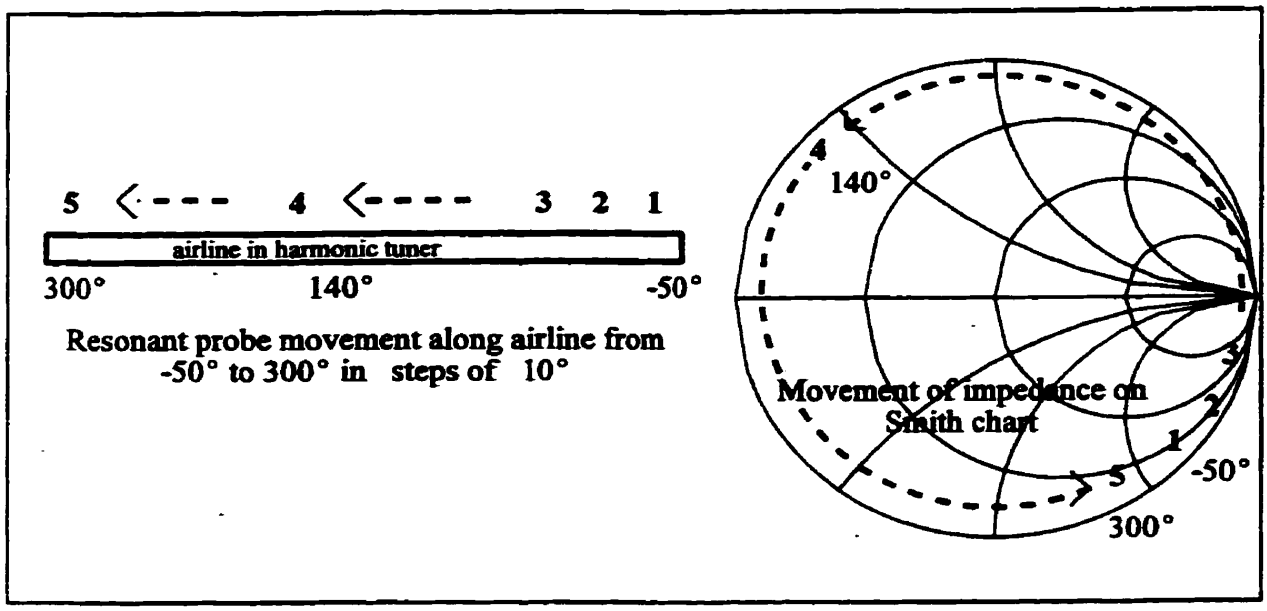


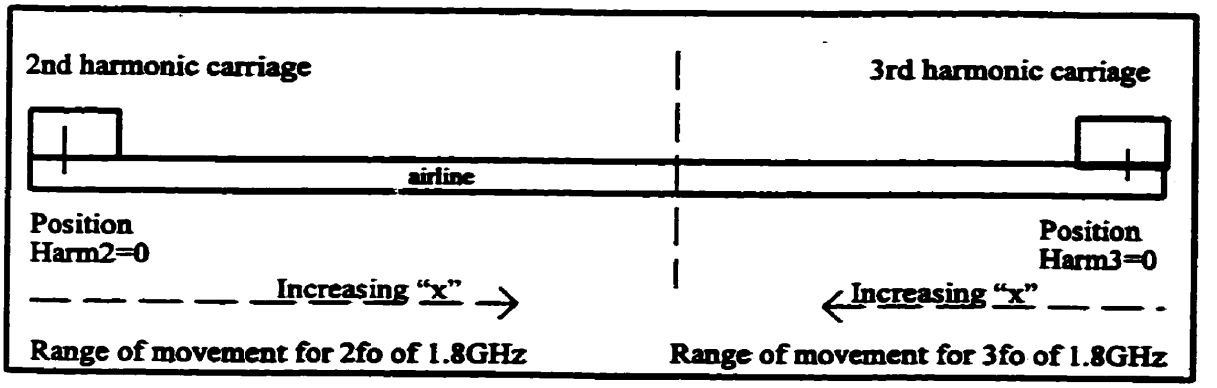
Figure 3.7 - Resonant Probe Movement with Resulting Impedances

There had been a problem initially where the probe reversed directions near the ends. This created problems in graphing and displaying the result. The software code was corrected during the course of the measurements to solve the problem.

Fig 3.8 shows the multi-harmonic tuner with both probes in the initialized (HARMx=0) position and the place, for this setup, where the initialized Multi-harmonic tuner impedances lie. The direction in which the impedances will move when "x" increases is shown. "X" is a stepper motor value used to indicate a place on the airline. The second harmonic resonator moves from left to right when leaving the initialized position, and therefore clockwise on the Smith chart (angles decreasing in degree value). The third harmonic resonator moves from right to left when leaving the initialized position and therefore counterclockwise on the Smith chart (angles increasing in degree value). The reason the second and third harmonic resonators are initialized at opposite ends is mainly due to the physical layout of the Multi-harmonic tuner tuner. There are micro-switches mounted on the end walls which the resonator carriages depress when

they reach there, indicating to the host system that the carriage has reached the x=0 position. The host system is aware of the carriage positions at all time and this switch provides a verification.

If, however, control is lost, due to perhaps program or computer re-initialization, the Multi-harmonic tuner will be initialised: the carriages will move until they depress the switches.



PHT

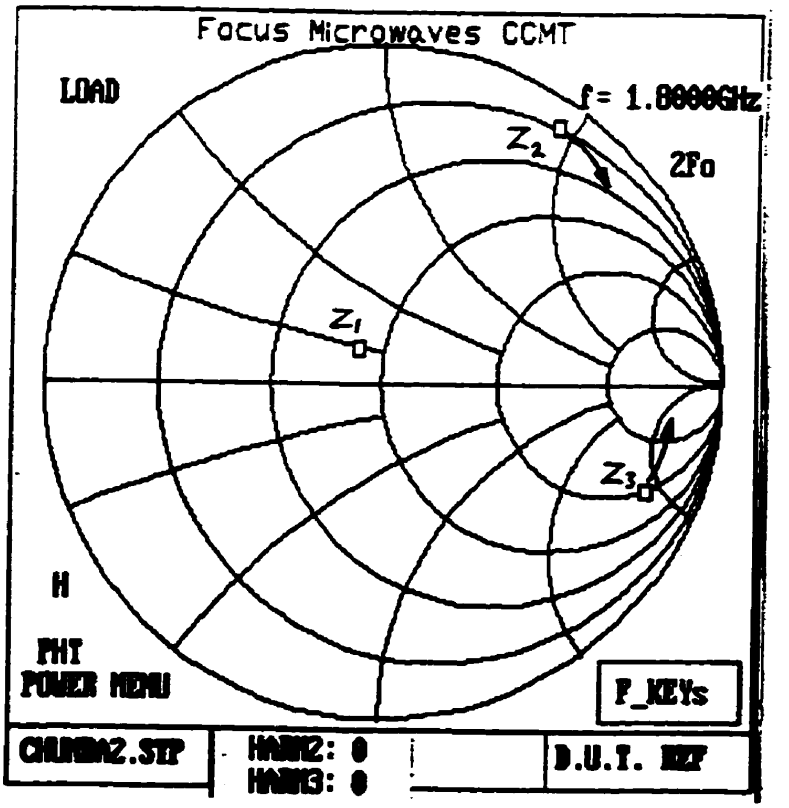


Figure 3.8 - Harmonic Impedances with PHT Initialized

3.6 - Inter Element Effects

As shown in section 3.1, each of the three resonant elements (fundamental resonator included) has an influence not only on the harmonic signal they are intend to tune, but also to some degree on the neighbouring ones.

Due to the physical order in which the stubs are presented to the travelling wave coming from the DUT, the 2fo stub can have an effect on the impedance at fo and 3fo since the skirt of this stub's response (which is a band reject filter) is non-ideal and presents about -15dB of reflection to adjacent harmonic signals. This can be seen in Figure 3.5 which shows the reflection coefficient of the Multi-harmonic tuner. It indicates about -15dB of reflection (return loss) at 1.8GHz. To be well adapted, a return loss figure of less than -20dB is expected. This shows the non-ideal nature of the two resonating elements. The return loss which the 2fo stub presents to the third harmonic and vice versa is difficult to measure since there is no measurement access. Both resonators are measured at the same time.

Note that the Multi-harmonic tuner presented here is the first one ever built and in view of these measurements, improvements have since been made to narrow the bandwidth of the resonant probes in order to lower the reflection on the neighbouring harmonics. This narrowing of the harmonic bandwidths, however, directly narrows the useful "fundamental" band. This is obvious because if the harmonic bandwidths go from 10% to 8%, then the usable fundamental bandwidth also reduces by this amount. In this work, the reflections for the harmonics of 1.75GHz and 1.85GHz have been adequate, so a narrower bandwidth could be afforded.

These two issues are mutually exclusive unless filtering

techniques are employed which can make the frequency response more "square". Such techniques are being developed by Focus Microwaves.

Measurements had been taken to determine the usable bandwidth of the Multi-harmonic tuner by measuring the magnitude of the reflection coefficient at the harmonics of various fundamentals. At harmonics of 1.6GHz and 2GHz they were deemed too low and at 1.7GHz and 1.9GHz, it was debatable. Thus 1.75 and 1.85 had been chosen to be sure of adequate performance. See Appendix A2.

Thus some correction and/or calculation is needed to account for the "broadband" impedance effects of physically and harmonically neighbouring elements. This effect is most prominent with the 2fo stub since it appears before the other two impedance devices physically, and because in frequency it is in-between and therefore closer to the other two.

The 3fo stub has a smaller affect on the fundamental signal since it is further away in frequency. It has a negligible effect on the 2fo signal since it is placed physically after the 2fo stub which has already reflected the 2fo harmonic signal back to the DUT.

The reflection from the fo and 3fo harmonic waves will also have an interference when travelling back to the DUT. For example, when the third harmonic signal is reflected off the 3fo stub it will be attenuated again by the 2fo stub (by the small amount of about -15dB) while on its way back to the DUT.

These attenuations are taken into account by the system during the calibration and S parameter operations.

The attenuations of each of the three harmonics is thus affected by 1)their physical order along the airline 2)the tuned frequencies of the elements, determined by the elements' dimensions

and materials; and 3)the losses in the transmission line which is dependent on a)the distance between the elements and the DUT and b)the distance between the elements and c)the dimensions and materials used.

Figure 3.9 is a measurement result showing the non-ideal nature of how the fundamental impedance component moves as the second harmonic resonator is moved (almost) 360° around the Smith chart. This occurs as the second harmonic resonant probe moves along its entire "x" range. Since the wavelength of the second harmonic is half as long as that of the fundamental, the fundamental component will sweep half as far as the second. The third harmonic will sweep 3 times as far as the first. Thus, as the third harmonic resonator is moved 360°, its non-ideal nature would see the its fundamental impedance component sweep along one third of the Smith chart.

A complication arising from this is that the fundamental impedance is not the same at either end of the 2fo tuning range, or the 3fo tuning range. So if the 2fo carriage abruptly changes from end to end of its "x" range, in order to change just a small number of degrees on the Smith chart (for example from -100° to -140° in figure 3.9), the fundamental impedance (due to the second harmonic resonator) will move a significant amount (almost 180°). The fundamental tuner itself will need to make a big change (correction) in its impedance in order to hold the overall fundamental impedance constant. This can potentially cause a discontinuity in the total fundamental impedance seen from resulting in a jump in the power and impedance during a harmonic sweep.

The trajectory of the fundamental impedance during a third harmonic sweep is shown in Chapter 4.

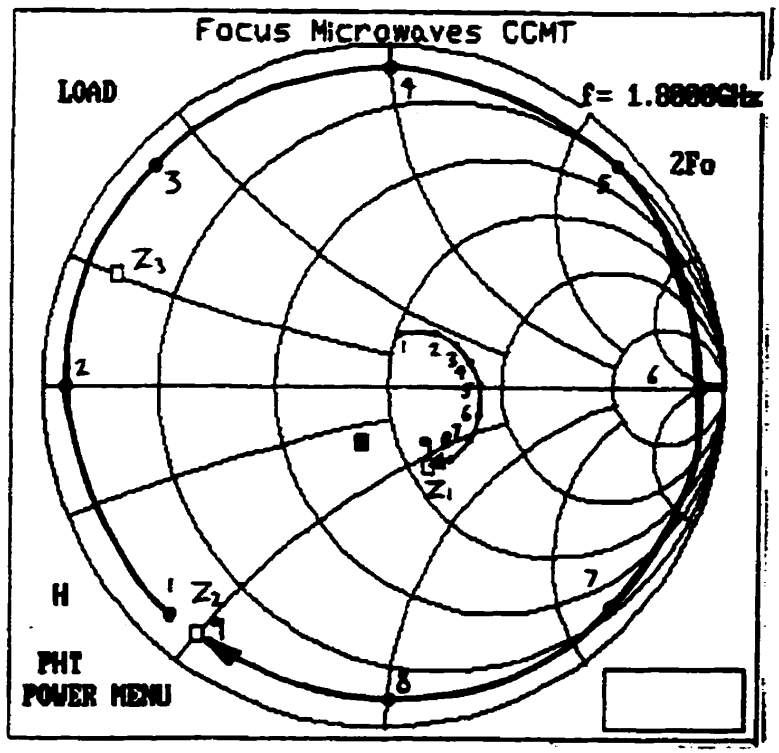


Figure 3.9 - Fundamental Impedance Trajectory (Z_1) During 2nd Harmonic Sweep

3.7 - "Fast" Multi-Harmonic Tuner Calibration

Measuring 100 physical positions of the Multi-harmonic tuner during calibration at each frequency takes about 20 minutes, depending on the network analyser used. Therefore the calibration sequence for three fundamentals (nine frequencies) will take about three hours. A "fast calibration" method has been developed to shorten this time.

The fast calibration is done such that the 2fo resonator moves to only ten positions while the 3fo resonator is in the initialised position and vice versa. This way, the calibration can be done with only 20 resonator positions per frequency instead of 100, decreasing

the calibration time to one fifth.

The effects the probe elements have on the neighbouring harmonics will still be accounted for because as long as the S-parameters of each tuner half is known at each position, they can be cascaded to give the S- parameters of the whole tuner. The task is to find the S-parameters of each half separately without having measurement access to the middle of the tuner.

This can be likened to a test fixture where measurement access to the centre of it, where the DUT resides, is unavailable, but through the TRL method both test fixture halves can be characterised so that the DUT reference can be de-embedded. In the case of the multi-harmonic tuner, which is actually two tuners side by side, the centre of it does not need to be as accurately "de-embedded" since it is not an important reference plane, so a TRL method is not necessary. As long as cascading the two halves accurately characterises the whole, it can be used in the setup. It is irrelevant whether "unused" portions of the airline in the centre region of the tuner are characterised with the left half or right half.

The multi-harmonic tuner used in this work is well suited to this type of calibration because at most operating frequencies, there is a large unused region in-between the two halves. This "extra" area becomes smaller when lower frequencies are used and the tuner halves require more of their airline to cover the half wavelength necessary to retain the full 360° tuning range.

To perform the fast calibration, the multi-harmonic tuner is first characterised on the network analyser, under host system control, in the initialized position. The result is placed in matrix "S_{TI}". This matrix is converted to the chain matrix so that it can be cascaded:

$$[S_{TT}] \rightarrow [T_{TT}]$$

Then the matrix is divided in two representing each tuner half:

$$[T_{TT}] = [T_{2fol}][T_{3fol}]$$

where $[T_{TT}]$ is the total matrix when initialized; $[T_{2fol}]$ is the initialised 2fo half and $[T_{3fol}]$ is the initialised 3fo half.

Each time the 2fo side is moved, (with the 3fo tuner remaining initialised), $[T_T]$ will be the new chain matrix of the entire tuner.

The new s parameters can be calculated from:

$$[T_{2fo}] = [T_T] \bullet [T_{3fol}]^{-1}$$

The T parameters are then converted to S parameters.

$$[T_{2fo}] \rightarrow [S_{2fo}]$$

This process is followed for each frequency and is repeated for the 3fo side.

CHAPTER 4

Setting Up and Verifying the Measurement System

4.1 Introduction

Measurements were taken with a through line installed, instead of any non-linear device, in order to verify the calibration and linearity of the setup and instruments. The setup appears in Figure 4.1.

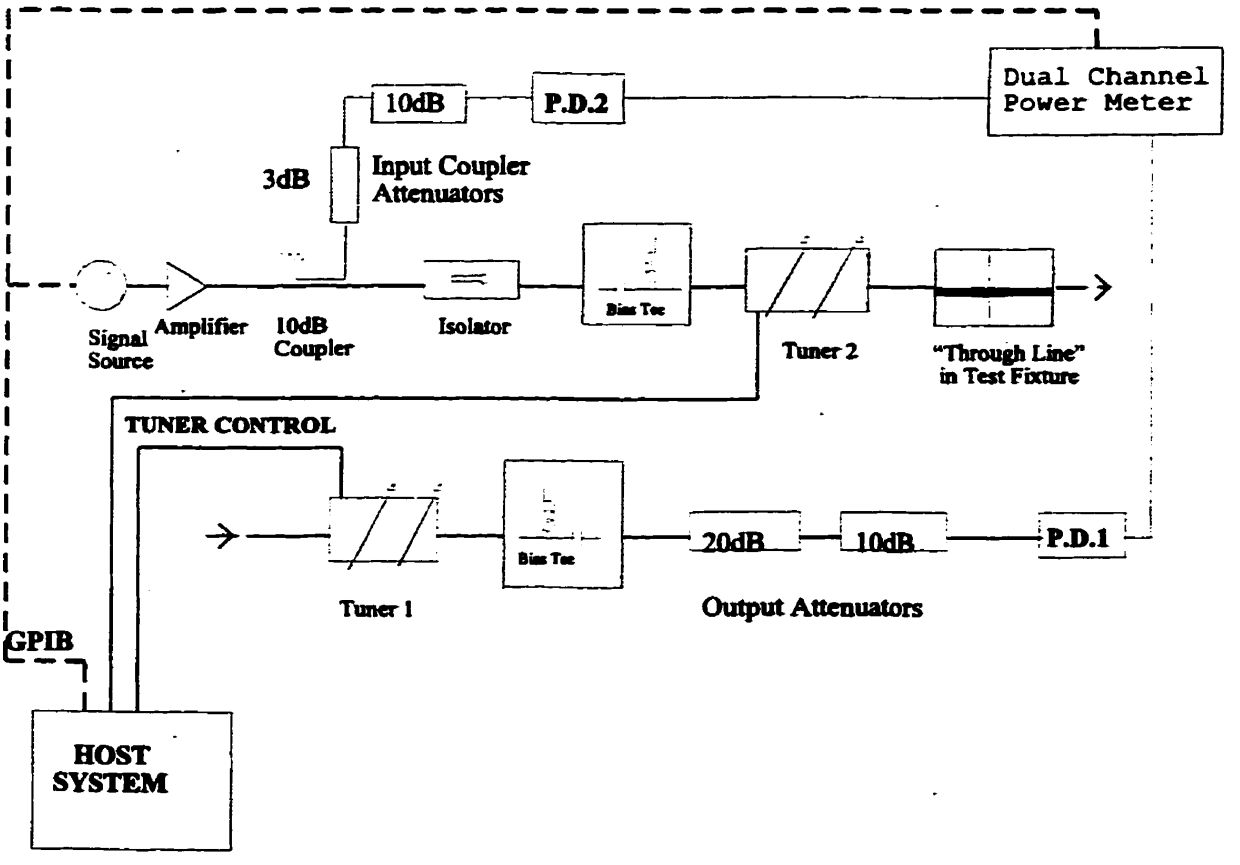


Figure 4.1 - Set Up with a "Through" installed in the Test Fixture for Set upVerification

4.2 Verification of the Set Up Using a Through Line

The through line was obtained by taping a gold strip across the test fixture gap, just as was done in the TRL "through" step. The setup appears in Fig 4.1. The verification was first done using tuners T1 and T2. The multi-harmonic tuner was installed afterwards. The following verification procedure was followed.

4.2.1- Step 1- Verification of the Impedance at the DUT Reference Plane

The first step is to check the characteristic impedance. Ideally, when everything has been well calibrated (including the network analyser) the input and output impedance seen from the DUT reference plane should be 50Ω when the tuners are initialized. Initialized tuners are 50Ω lines which do not create any reflections. This ideally results in the source and load impedances falling onto the middle of the Smith chart. Usually the impedance markers, displayed on the screen, will fall a little bit off from the Smith chart centre. A $|\Gamma| < 0.05$ is considered good. This verification is done for all the fundamental frequencies at which the setup and tuners were calibrated.

No measurement is taken and no signal is injection at this stage. Just the data which was obtained during calibration is verified. In fact, no set up is actually needed at this stage because it all takes place "inside the computer". Inaccuracies appearing at this point (off centre impedance markers) are due to inaccuracies that occurred during calibration, such as measurement errors, VNA standards tolerances, connector VSWRs, connection inconsistencies, GPIB errors, etc. Errors that are "completely off" can be due to file handling errors (though rare), system configuration mistakes (such as the wrong set up file being enabled,

etc). The impedance can also be displayed at the reference plane of the tuners and the test fixture. Checking the impedance at other references can provide insight and quick troubleshooting help for the setup.

It is beneficial during calibration to look over newly created data files and to evaluate whether the result is satisfactory, if it should or can be made better. It is easier to re-attempt a calibration step when it is still connected to the network analyser than when it is screwed into your setup. For best accuracy, the network analyser should be carefully calibrated just prior to tuner and set up calibration. Tuner calibration is critical because high reflection factors come into play (high VSWRs) which require high accuracy of the network analyser instrument.

4.2.2- Step 2- Verification of the Gain and Linearity

This step is to verify that 1)there is no setup gain or loss- which means that the setup losses have been accurately accounted for by the host system that 2)the source power is adjusted for the required range and that 3)the power detector probes are linear over the required dynamic range and frequency. Since power is being dealt with, these are real, and not complex measurements.

A signal is injected into the setup and the output is verified. The PD2 reading is inserted into equation 2.10, shown below. This equation refers the measured input power to the DUT input reference plane. The PD1 reading is inserted into equation 2.8, repeated below. This equation refers the measured output power to the DUT output reference plane. The two DUT reference plane values should be equal because a through line is being dealt with which has the same power on both sides.

$$P_{in}(DUT) = P_{out}(DUT)$$

$$PD2 + L_{13} - L_{BT2/Iso} - L_{T2} - L_{I/P\ fixt} = PD1 - L_{Att} - L_{BT1} - L_{T1} - L_{O/P\ fixt} \quad (4.1)$$

The system calculates these values upon request and reports the input power, output power and power gain. The injected signal power level should be varied between the levels that will be used during measurement.

The goal of this exercise is to verify that the linearity and dynamic range of the power detectors is adequate for the upcoming transistor measurements. For the 3W MESFET used for most of this work, the required transistor input power will be between 10 and 25dBm. The output power detector will have power levels of about 15dB higher than this, due to the gain of the transistor. It would therefore require test power levels from 25 to 40dBm. Therefore, an input power sweep from 10 to 40dBm would cover the requirements for verifying both power detectors. However, the attenuators preceding PD2 were not large enough to protect the PD2 power detector from the extra 15dB, so removing the 20 dB attenuator from the output block and performing only the 10 to 25dBm sweep was the best compromise solution during this test procedure.

One must be very cautious about not exceeding the maximum power levels of the detectors lest they become over-heated and damaged. This could incur considerable expense and erroneous measurements. "Worst case" attenuation must be placed in front of the "power heads" at all times and the signal generator must be limit programmed- given a level which it will not exceed even if it receives a command to do so from the GPIB or front panel. Power detector probes, like most transducers, operate most accurately in the middle of their range and should be operated there when possible. This also provides a safety buffer.

Once everything is in place the power can be applied and the zero gain can be verified at the low medium and high levels. Many elaborate load pull systems, such the one being employed, can perform power sweeps and display the plot of the input verses the output power. This shows the dynamic range and linearity performance directly. Fig 4.2 is an example. It is important, obviously, to set the upper limit of the power sweep, as well as the upper limit of the generator.

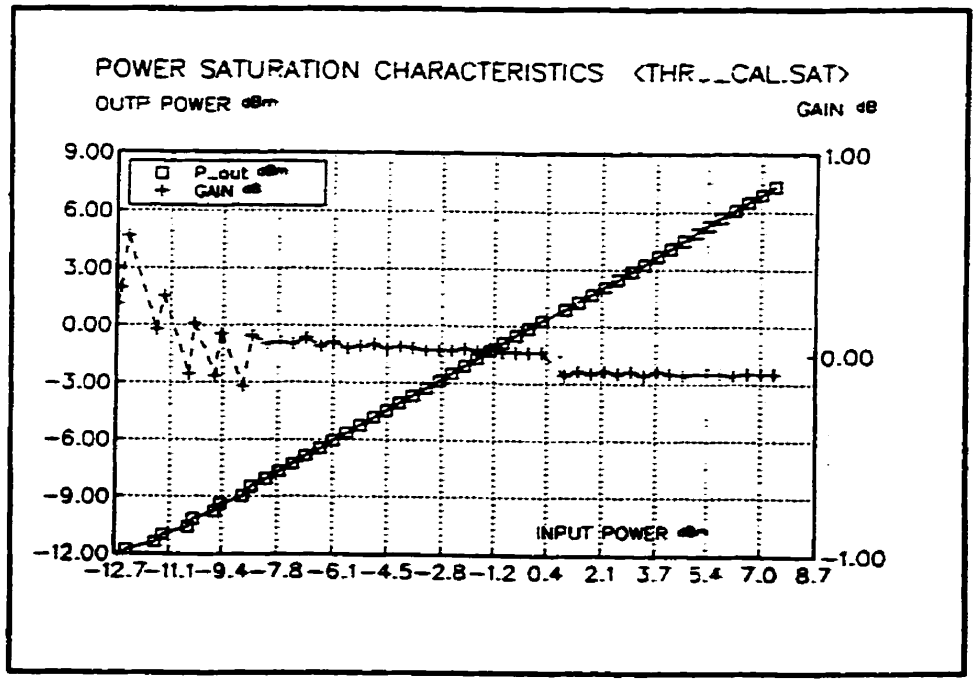


Figure 4.2 - Gain and Power Linearity Verification

This test must be done for all the fundamental calibration frequencies. For the 3W MESFET this is at 1.75, 1.80 and 1.85GHz.

On first pass, the linearity and gain were not acceptable.

Depending on the frequency being used, the gain was about 0.1dB at the low power end and 0.2dB at the high power end. Upon placing the power probes, one after the other, at the same point in the circuit it was discovered that PD1 was reading about .2dB higher than PD2 in the upper power range being used. A correction was made in the system file which accounts for the calibration factors of the detector probes. Normally, the calibration factor information which is marked on the probe itself by the manufacturer is copied into this file. In this case, something had changed, perhaps due to excessive power being absorbed by the probe at some point in its life.

4.2.2.1 - Power Detector Probe Calibration

Each probe is screwed into the 0dbm, 1KHz reference of the power meter (Boonton 4200). The variation from 0dBm is written into the first line of the file. The frequencies with their corresponding cal factors are written into the following lines of the file. This is the information marked on the probe itself. For each power measurement the system adds the reading, the first line and a cal factor. However, different power meter manufacturers have different ways of approaching the calibration factor issue.

To provide a finer calibration, cal factors were added at the specific frequencies used: 1.75,1.80,1.85GHz. The cal factors were measured by screwing the probes directly into the signal generator and using the level and frequencies displayed on its front panel. This instrument was trusted (HP8648C) as the calibrating instrument. This is less expensive than sending the probes to get calibrated at a certified lab. The PD1 cal factors remained unchanged from what was marked on the probe itself, so the signal generator was verified in this way.

It was the PD2 cal factor which was changed from -0.2 to +0.01. This probe was also not linear across the range, reading about 0.1dB too low in the low power range and 0.1dB too high in the high power range. This new cal factor was applied at the level the probe would be reading when the transistor is operating in its upper wattage range. This level was around 6dBm and is where the most accuracy is needed. This calibration was checked two weeks later and PD2 needed to be calibrated again. From this it was concluded that this probe is about ±0.1dB accurate.

After increasing the calibration factor of PD2, effectively increasing the input power by about 0.2dB, the gain became about 0.2dB negative. In order to compensate for this, about 0.2dB of attenuation was trimmed from the input coupler attenuator file. This brought the gain to an acceptable ±0.05dB. This was done at each of the three frequencies.

4.2.3- Step 3- Verification of the Tuner Calibration

In order to verify the tuner calibrations, a "through line" load pull is performed. This graphically displays the output power, for a constant input power, as the tuner is moved to each of its 361 points. Upon displaying the load pull result it was seen that there was a discontinuous "spike" in the tuner calibration and that it had more power (less loss) on the right hand side of the Smith chart. See Fig 4.3.

These errors were attributed to network analyser issues. The spike is reported as an occasional problem with the HP8753D network analyser. It allegedly reverses the S_{21} phase, for a reason unknown, and this affects the loss stored in the tuner

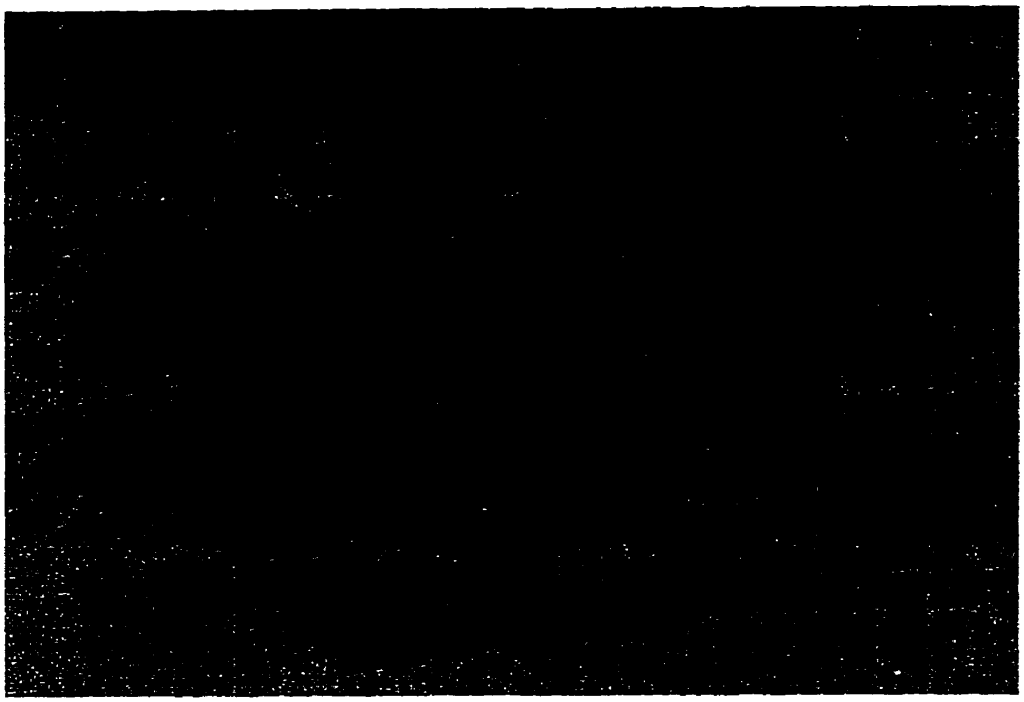


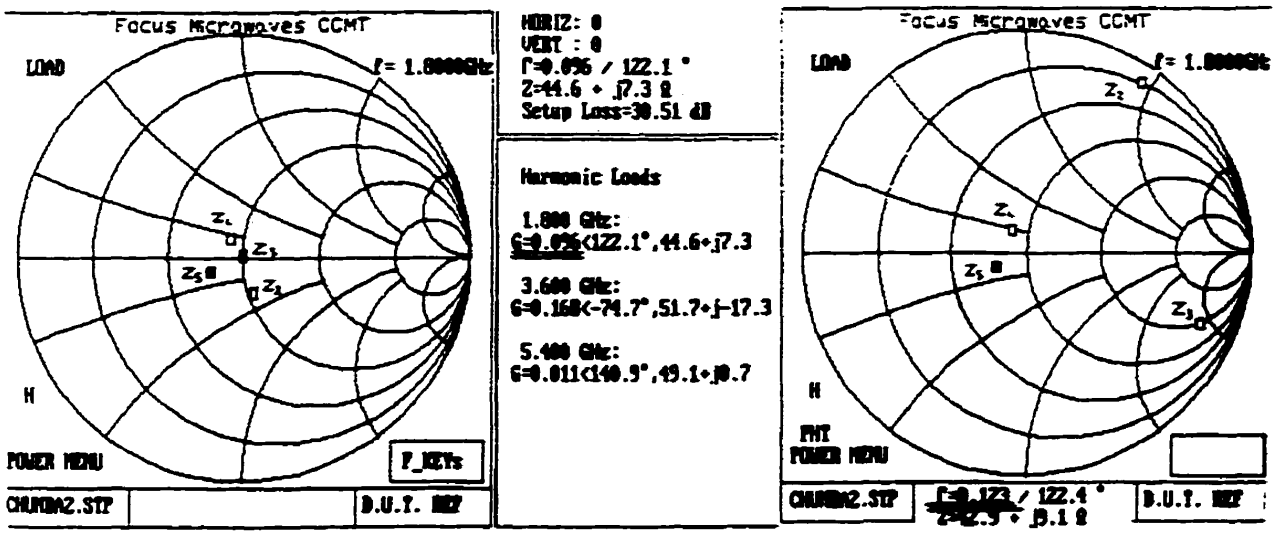
Figure 4.3 - Bad "Through Line" Load Pull Result

calibration file for those tuning points affected. The "Leaning to the Right" problem is attributed to an old VNA calibration being used to calibrate the tuner. This illustrates the importance of a careful network analyser calibration prior to a tuner calibration. A new VNA and tuner calibration was performed.

4.2.4 - Step 4 - Installing the Multi-Harmonic Tuner

The multi-harmonic tuner was installed and its tuner calibration file was enabled. This file is needed so that the system can account for the new tuner in the overall impedance and power calculations. Once installed and the previous three steps are re-verified:

Step 1 - Verification of the Impedance: The new tuner will drastically increase the reflection coefficient at the harmonics. This is shown in Figure 4.4 for 1.8GHz.



Before **After**

Figure 4.4 - Verification of Impedance before and after Multi-Harmonic Tuner Installation

It also shows that $|\Gamma_{Lfo}|$ (Z_L in the figure) has increased from 0.096 to 0.123. This is due to added reflections at the fundamental due to a non-ideal (non-zero) S_{11} parameter in the fundamental band. This is shown in Figure 3.5. This is due to the non-ideal response of the resonant probes and to connector and airline tolerances. This can change and possibly increase, as in this case, the magnitude of the reflection coefficient seen from the DUT. This measurement was also done at 1.75 and 1.85GHz and is shown in the Appendix A3.

It should be kept in mind that each of these impedance points

is actually on a different Smith chart, but they are all superimposed onto one chart for simplicity. There is one input and three output Smith charts. The input is unaffected by the multi-harmonic tuner insertion.

Step 2 - Verification of the Gain and Linearity: The gain of the set up should still be zero. This means that the system has accurately accounted for the losses of the new tuner. The linearity of the power detectors are not affected by this tuner installation.

Step 3 - Verification of the Tuner Calibration: An illustration of the impedance points of the multi-harmonic tuner at the harmonic frequencies is shown in Fig 3.2 and 3.3. It is a good idea to perform new "through line" load pull at the fundamental frequencies. The output power will be the same since the output power is represented at the DUT reference plane, but the plot will look taller due to the maximum magnitude of the reflection coefficients being slightly reduced by the insertion loss of the multi-harmonic tuner.

4.3 - Verification of Both Tuners

4.3.1 - Verification of P_{OUT} for Increasing $|\Gamma_{Lfo}|$ During Phase Sweeps (using a Transistor)

A test which was performed in the early stages of this project, with a transistor installed, was to vary the magnitude of the fundamental reflection coefficient, $|\Gamma_{Lfo}|$, and see what effect it had on output power variations during harmonic sweeps. The $|\Gamma_{Lfo}|$ was set at 0.5, 0.6 and 0.73 respectively with a phase angle, $\angle\Gamma_{Lfo}$, of 270°. At each magnitude the harmonic phases were swept individually and the output power, P_{out}, for each of these sweeps was recorded and plotted. As seen in the results shown in Figure 4.5 for each second harmonic sweep, the higher the magnitude of the fundamental reflection coefficient $|\Gamma_{Lfo}|$, the greater the variation in the output power during the phase sweep. This is especially apparent when the magnitude has reached 0.73. The same was observed for the third harmonic. (The y-axis values are higher than they were in reality because of a missing attenuator in the output block. This is not important since it is only the variation that is of interest here.)

At a reflection coefficient, $|\Gamma_{Lfo}|$, of 0.73 the power variations during the second and third harmonic sweeps were about 2¼dB and 1¾dB respectively. This is higher than what has been predicted [4,5,7] and therefore the results looked suspicious. At a reflection coefficient of 0.6 and lower the power variations were more comparable at about 0.5dB. This led to the decision to limit the magnitude of the reflection coefficient to 0.6 during the first transistor measurements. Higher reflection coefficients would be utilised once more investigation and development work had been applied to the multi-harmonic tuner and software. A quarter wave transformer could also be installed on the test fixture then which would reduce the maximum reflection coefficient.

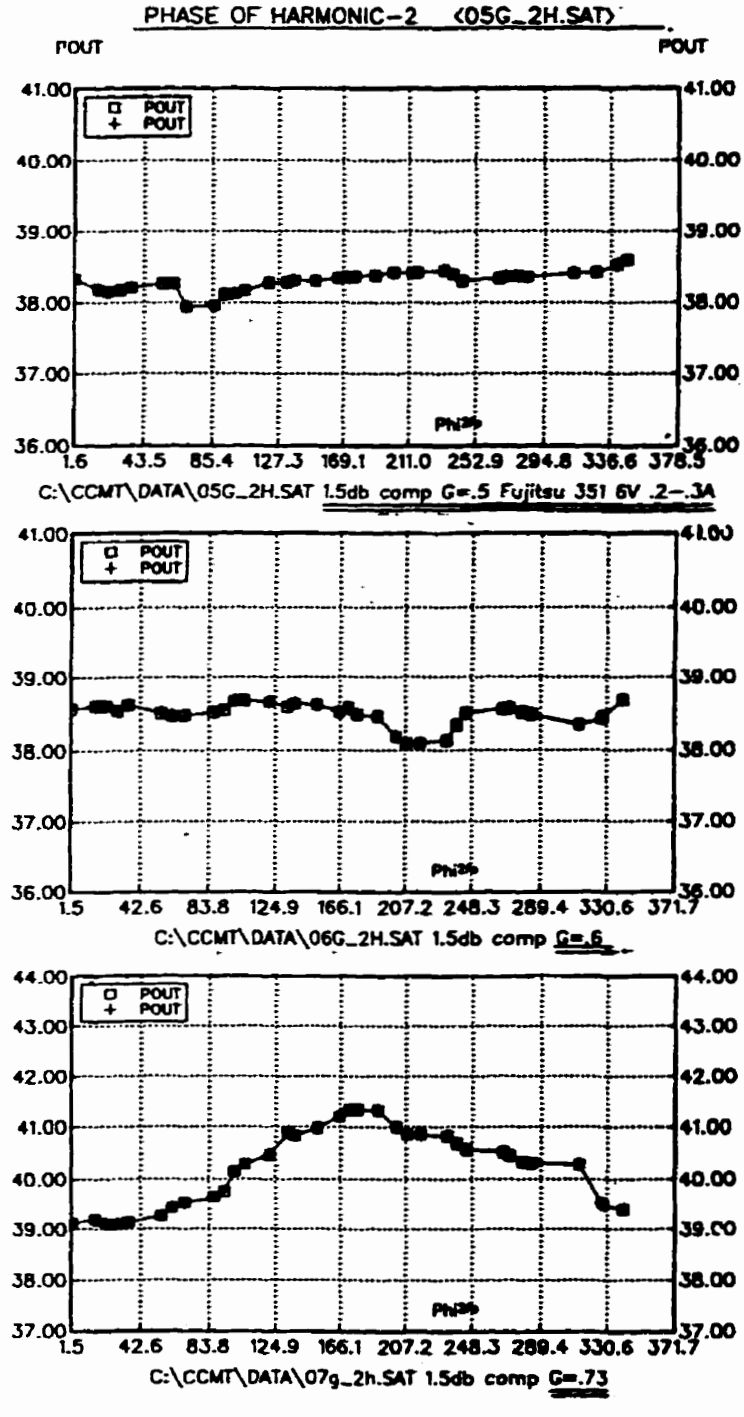


Figure 4.5 - Output Power During Phase Sweep for Increasing Fundamental Reflection Coefficients (using a Transistor)

4.3.2 - P_{out} Variations During Second Harmonic Phase Sweeps at Increasing Fundamental Phase Angles, $\angle\Gamma_{Lfo}$. (using a Through Line)

In the following investigation the magnitude of the fundamental reflection coefficient , $|\Gamma_{Lfo}|$, was kept constant at 0.6, as decided in the last section, and the phase, $\angle\Gamma_{Lfo}$, was moved 45° further after each second harmonic phase sweep. This exercise was to investigate if there is an optimum phase of the fundamental reflection coefficient where the fundamental impedance is more stable and the output power would vary less. In theory, there should be no variation of power since a through line is used and because the magnitude of the reflection coefficients do not change.

It was highly suspected that correcting the fundamental impedance is more difficult when the harmonic tuner changed from one end of its tuning range to the other. When this occurs, the fundamental tuner needs to make a bigger change than usual to compensate for the impedance change incurred from the resonant probe moving from one end to the other between measurements. Any test instrument will lose accuracy in performing a fine tuning operation when there is a big change taking place. Most of the big jumps seen in the plots of output power verses harmonic phase occur when the harmonic resonator moves from one end of its tuning range to the other, taxing the stability of the fundamental impedance.

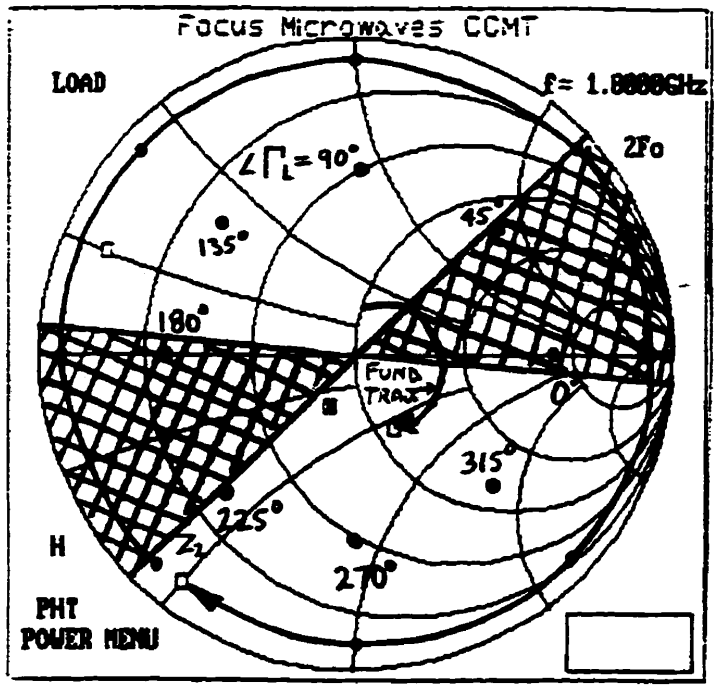


Figure 4.6 - Fundamental Impedance Trajectory During 2nd Harmonic Sweep

Aside from this more obvious correction difficulty, it had also been noticed that at some angles of the fundamental there were less variations, even when the harmonic resonator moved from end to end. There is also some inspiration gained from looking at the fundamental impedance as the second harmonic is swept. See Figure 4.6. Perhaps it was best when the angle of the fundamental reflection coefficient is at mid-angle of this fundamental impedance trajectory, as shown by the shaded area.

The results of the output power for eight fundamental impedance angles, ∠0° to ∠315°, during second harmonic sweeps, appear in Figure 4.7. It can be deduced from these plots that the smoothest outputs are indeed those which are "broadside" to the fundamental impedance trajectory. This is easier to conclude from when looking at the 0° to 180° plots than from the 180° to 315° plots but even there the trend does exist. Observe that the y-axis

scale (P_{OUT} in dBm) is not consistent throughout the plots, and this makes the smoothness a little harder to see.

Perhaps, for some reason, the fundamental impedance is more stable at this angle because as viewed on the Smith chart, the impedance corrections that are required are more circumferential than radial. Electrically, this means that the corrections are more reactive than real. In a passive system making real corrections where the magnitude of the reflection coefficient is high is more difficult due to the difficulty in working accurately with real losses near the maximum reflection coefficient. The resonant probe of the fundamental tuner is already very close to the central conductor in the airline so the resolution is lower. Reactive changes are more easily accomplished because they involve only a lateral (linear) movement. The magnitude of the reflection is here 0.6, out of a maximum of between 0.75 and 0.85, which is approaching the maximum.

Another factor is that as the harmonic tuner performs its sweep, the vectorial component at the fundamental can "pull" the maximum reflection coefficient to a lower value, giving the fundamental tuner less "room to move" during corrections. It can be explained from Figure 4.6 and 4.7 that a fundamental reflection angle around 90° and 135° will have the biggest disadvantage, explaining the least smooth plots. On the other side, near 270° and 315°, it can be explained that this disadvantage is lower, hence showing a smoother result.

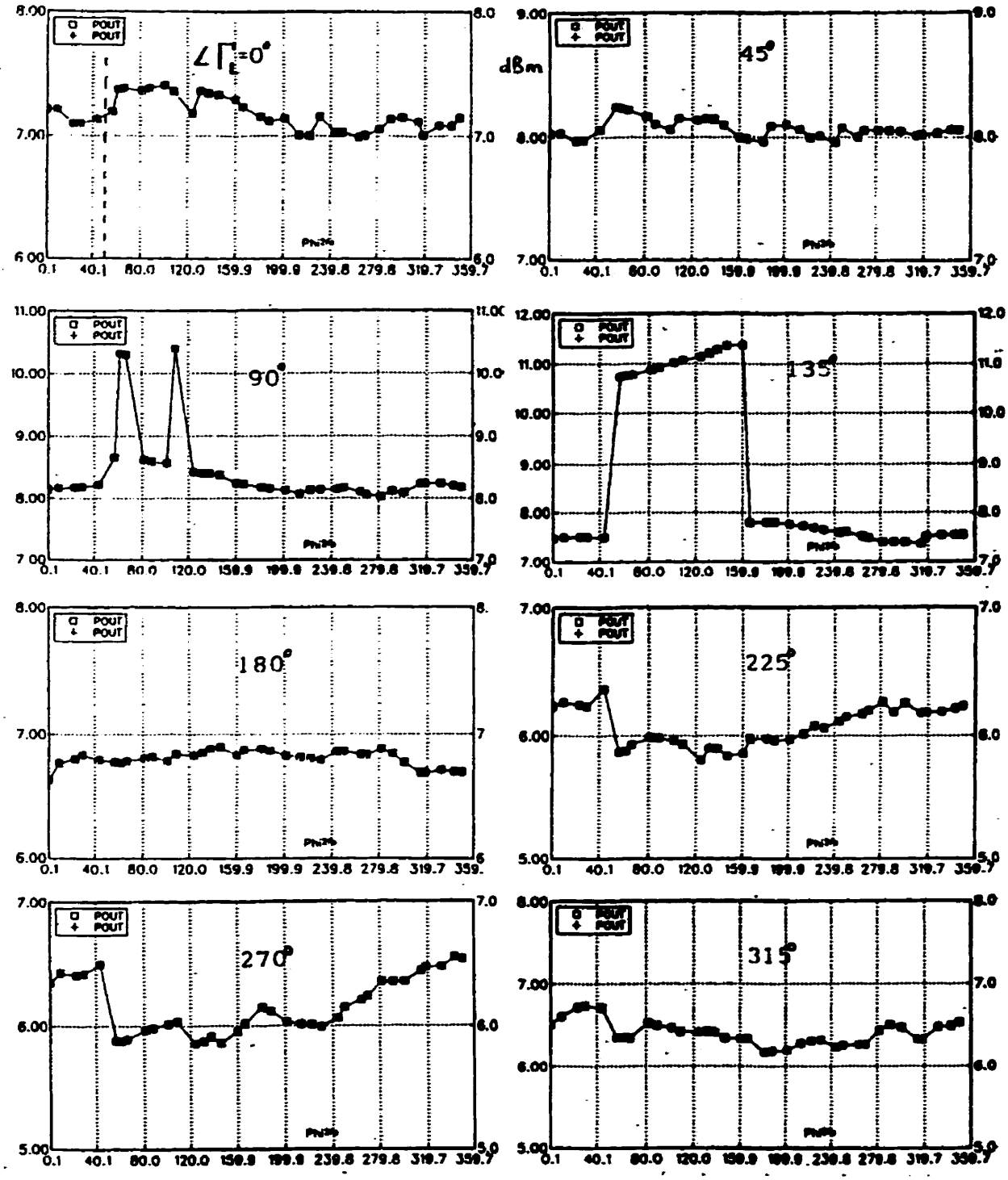


Figure 4.7 - Output Power During Second Harmonic Phase Sweeps at Various Fundamental Phase Angles (using a Through Line)

Since the distance of the stub resonator from the DUT corresponds to the phase, (which is the basic mechanism of the harmonic tuner) it suggests that the harmonic tuner can be placed at a certain physical distance from the test fixture which will optimize its performance in the setup. A procedure that can be followed is :

1)the desired fundamental impedance can be chosen from tests performed with the transistor and the fundamental tuner only. This is done in Chapter 5 and then

2)the harmonic tuner can be installed and, temporarily replacing the transistor with a through line, be varied in order to locate its optimum distance from the DUT reference, as was done here. Then

3)once the harmonic tuner has been placed at its optimum distance, the transistor can be reinstalled and harmonic fine tuning can commence. This is done in Chapter 6.

Airlines can be used to move the harmonic tuner to the optimum distance. The issue is to put the angle of the fundamental reflection coefficient roughly broadside to the fundamental impedance trajectory during the second harmonic sweep.

It is more important to do this for the second harmonic sweep than for the third harmonic sweep since more performance can be gained from second harmonic optimization. It can only be hoped that the fundamental impedance that will be used will also fall broadside to fundamental impedance trajectory during the third harmonic sweep. This was, however, not tested. The physical segments on the airline used by each harmonic tuner are not, as of yet, separately adjustable, so the location of the third harmonic segment is dependant on the location of the second.

As a result of these studies, the software and hardware have since been modified to improve the output smoothness. The results were too premature at the time of this writing.

4.4 - Verification of the Fundamental Impedance Stability During Harmonic Tuning Using a Network Analyser Instrument

The harmonic and fundamental tuners were connected to the network analyser as shown in Fig 4.8. All devices were under host system control.

The fundamental tuner was tuned to $\Gamma_L \approx 0.72\angle 180$ as seen from

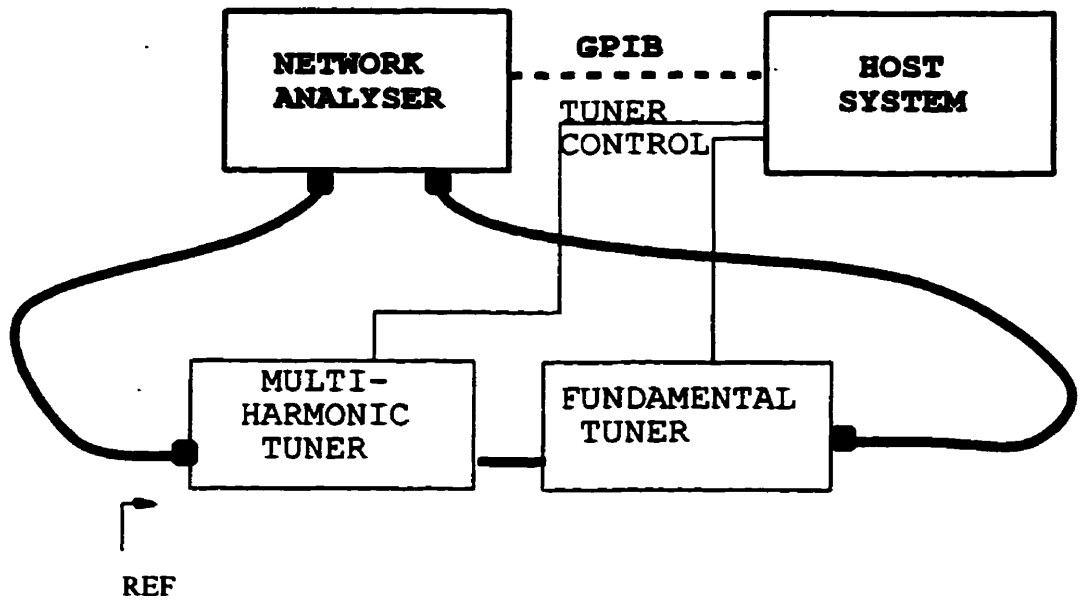
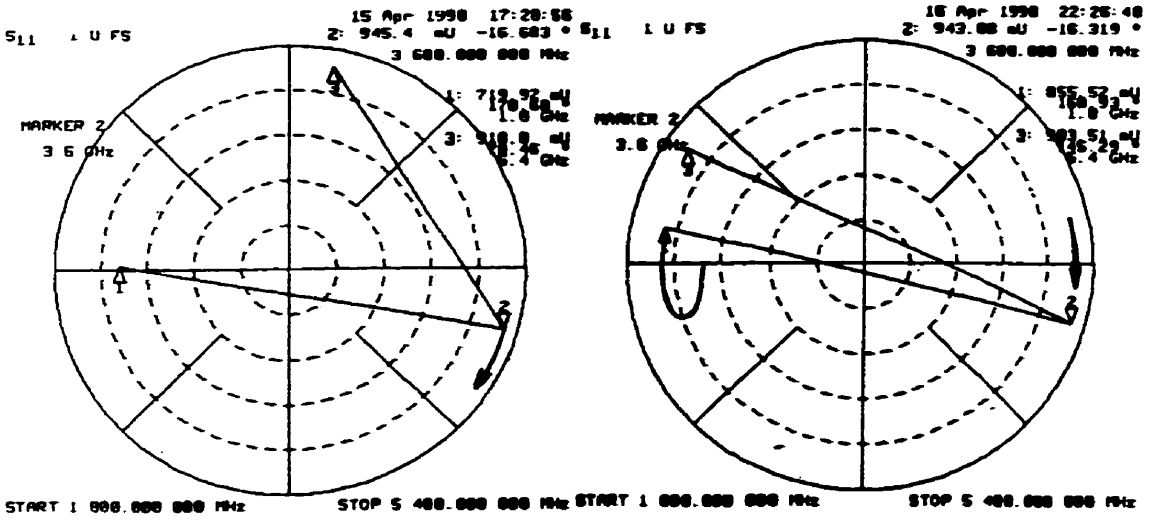


Figure 4.8 - Tuner Setup Verification using the Network Analyser

the reference plane of the left hand connector (APC-7).

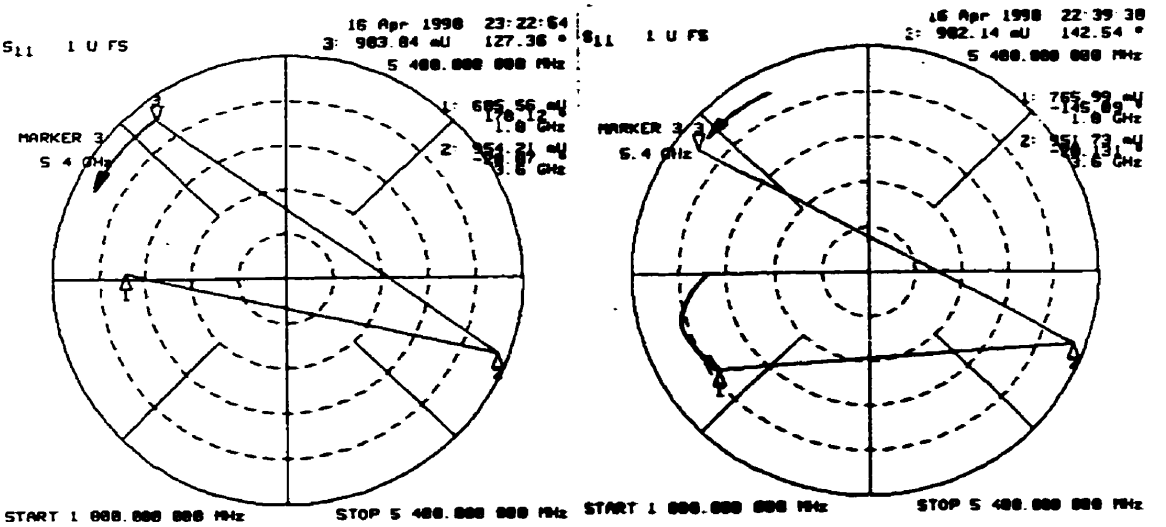
360° second and third harmonic sweeps were performed in order to see how well the system was able to hold the fundamental impedance constant under these changing conditions. Then the correcting software was disabled for the same sweeps in order to establish how much the fundamental impedance would move. The summary of the result appears in Figure 4.9. Frame by frame illustrations for each of the four cases can be found in Appendix A4-A7. Marker 1,2 and 3 mark the first (fundamental), second and third harmonic respectably.

With the correcting software enabled the fundamental impedance is very stable, seen in the two left hand side figures. With this software disabled during the sweep, the fundamental impedance moves approximately 30°, as seen by the "fundamental impedance trajectories" on the two right hand side figures. This is how the fundamental impedance would move if it wasn't for the fundamental impedance correcting function. It is a significant amount. This movement is caused by fundamental impedance component of the second and third harmonic resonant probes. Techniques are being developed to reduce this component.



Correcting Software Enabled (Stable Fundamental Impedance) **Correcting Software Disabled (Fund. Impedance Trajectory)**

a) Second Harmonic Sweep



Correcting Software Enabled (Stable Fundamental Impedance) **Correcting Software Disabled (Fund. Impedance Trajectory)**

b) Third Harmonic Sweep

Figure 4.9 - Fundamental Impedance Stability During Second and Third Harmonic Sweeps

It is surprising how much the fundamental impedance changes during the third harmonic resonator sweep (Figure 4.9b). It would be expected that this change is much less than that caused by the second harmonic resonator sweep knowing that its tuned frequency is further.

What can also be seen is the movement of the third harmonic impedance as the second harmonic sweep is executed (Figure 4.9a). This is because the third harmonic resonator resides after the second one.

What can also be established is that during the second harmonic sweep the fundamental impedance traces something like a half circle and for the third harmonic sweep it traces something like a third of a circle. This is in accordance with basic theory.

From this measurement it can be concluded that the desired fundamental impedance can be held constant at this reflection coefficient. Since this measurement was performed on a network analyser (HP8753D), it also validates to a large extent the impedance tracking performance of the host system. Also, since the magnitude of the reflection coefficient is 0.7, the system should perform even better at a magnitude of 0.6.

It is known from some past works [14,22] that the optimum fundamental impedance of the 3W MESFET to be used also lies near $0.7\angle 180$, but this is as seen from the DUT reference plane and not the tuner reference plane as was measured here. By comparing the orientation of the fundamental impedance trajectories of Figure 4.6 (DUT reference plane)and 4.9 (tuner reference plane), it can be seen that the two reference planes are about 270° apart. Hence this area represents about 270° from the DUT reference.

CHAPTER 5

Transistor Measurements at the Fundamental

5.1 - Introduction

The transistor (a 3W MESFET) was inserted into the test fixture (containing 50Ω lines) and the fundamental tuner was used to synthesize the output impedances (the multi-harmonic tuner was not installed). The second and third harmonic impedances are known and displayed by the system but are not controllable by this tuner. Varied were the DC bias, RF compression, frequency, performance goal and transistor sample. The results are tabulated and presented.

At each bias point and compression level the output impedance was tuned for the highest power, efficiency, or power/efficiency compromise. The goal of these fundamental load pull measurements is to find a source/load impedance and dc bias for obtaining a very good compromise between the transistor's maximum power and maximum power added efficiency (PAE) that could be fabricated on a microstrip substrate using passive elements. The harmonic impedances are not controlled and left as they are, as would be the case if a fundamental termination were built on a microstrip circuit. This represents a situation closer to reality than if they were specifically adjusted to 50Ω, as in some load pull setups. The fundamental tuner does, however, present an impedance close to 50Ω to neighbouring harmonics as can be seen in Figure 4.4. The same is true for a resonator stub type termination in a microstrip design.

As predicted by theory [5,6], the best compromise between output power and efficiency was found with a class AB bias point. Other biases were also tested.

The optimum load impedance was near 0.7∠175°. The optimum source impedance was near 0.8∠180°. The optimum impedance was found to change with bias, compression, and the transistor sample.

Seven dc bias points were tested. The results appear in Appendix B. The output power compression was varied between 0, 1 and 2dB and two transistor samples were used before arriving at the final choice of bias. This choice was I_D=200mA and V_{DS}=8V

More concentration was given to the centre frequency of 1.8GHz though the other band edge frequencies of 1.75 and 1.85GHz were tested before arriving at the final choice of impedance. Two transistor samples were used. The final load impedance chosen was 0.6∠174°.

The input impedance was also tuned to its optimum value throughout the measurements and its final value was chosen to be 0.8∠180°. Its impedance is far less critical to the output performance as has been reported [18].

5.2 - File Names of the Measurement Results

Files were used to hold the measurement results. Each file contains measurement results for a given input impedance, output impedance, dc bias, compression, frequency, transistor sample and performance goal. Test conditions are given inside the file, but are also saved in the file which is named after the test conditions themselves. The following is an example:

Measurement filename: F 1 C0 B1 P R . 001

F - Sample 1 of the transistor, Fujutsu FLL351ME
- **G** the second sample had been used and
- **H** third sample was used

1 - The frequency was 1.75GHz
- **2** 1.8GHz
- **3** 1.85GHz

C0 - No Compression - input level about 3dB below onset of compression
- **C1** Compression = 1dB
- **C2** Compression = 2dB

B1 - Bias point 1 = 10V, 500mA (V_{DS}, I_D)
- **B2** Bias point 2 = 6V, 600mA
- **B3** Bias point 3 = 3V, 900mA
- **B4** Bias point 4 = 3V, 200mA
- **B5** Bias point 5 = 10V, 200mA
- **B6** Bias point 6 = 8V, 300mA
- **B7** Bias point 7 = 8V, 200mA

P - The input and output impedance are optimized for maximum power
- **E** The impedances are optimized for the goal of max PAE
- **B** A compromise has been made between power and efficiency

R - The "reduced" reflection coefficient. The P, E or B output reflection coefficient is taken and its magnitude is reduced to 0.6, using the same angle. This ensures more stability during subsequent harmonic tuning (as discussed in Chapter 4).
- **no R** The reflection coefficient is not changed from optimum

001 - first measurement pass if more than one was performed, they can be stored in different files or appended.
- **002** another set of measurements under the same test conditions.

The files are in the text format. The following is an example of the contents of such a file:

---

measurement filename= F2C1B1E.001

Result of direct Peak Search

Tune LOAD, P-inp=17.55 dBm
10.0/395.74/1.2/2.8081
Setup File = CHUMBA1.STP
Operation File = T1101800.COR

Frequency = 1.800 GHz
Γ-source = 0.879 / -179.5ø
Γ-load = 0.672 / 166.8ø
Maximum Efficiency = 50.6%
Z-Source = 3.22 + j-0.24 Ohm, Z0(S)=50.0 Ohm
Z-Load = 9.95 + j5.56 Ohm, Z0(L)=50.0 Ohm

Harmonic Impedances:

Source Impedances

Frequency = 3.600 GHz: Z=6.93+j12.27 Ω
Frequency = 5.400 GHz: Z=132.47+j95.32 Ω

Load Impedances

Frequency = 3.600 GHz: Z=29.91+j40.07 Ω
Frequency = 5.400 GHz: Z=83.21+j-19.11 Ω

5.3 - Choosing the Transistor bias points

The bias points tested cover a variety of regions on the transistor's I_D vs. V_{DS} output plane. They are shown in Figure 5.1. The dc bias point (which is also referred to as the dc polarization, quiescent point or Q point) is established without any RF power flowing through the device. This is because the RF signal almost always increases the average DC drain current and it would be difficult to establish a repeatable DC bias. Using only the DC power supply provides an easily referable point, and a true

"quiescent" point, on the static load line so that comparisons can be made. These are the points shown on the graph of Figure 5.1. During measurement runs, the RF can be turned off at any time to ensure that the intended Q point is still applicable. DC bias point drift occurred occasionally when the transistor was warming up from ambient; and when it was running at powers above 2W, where the increased power dissipation likely raised the temperature too high.

The power and efficiency results at each bias point are summarized in Table 5.1. In each case the impedance, which may

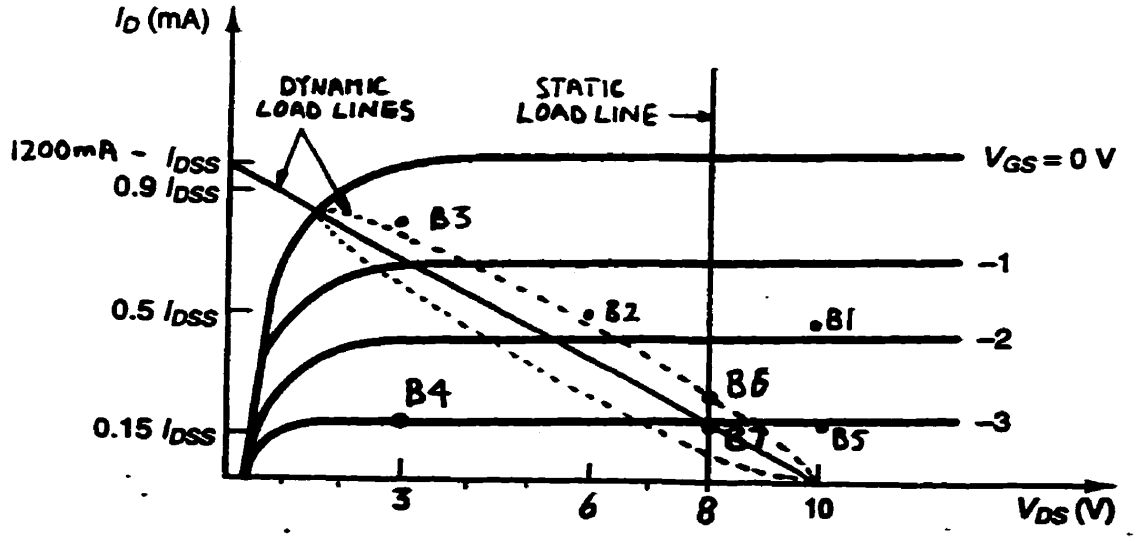


Figure 5.1 - GaAs FET Output IV Characteristics with Tested DC Bias Points and Load Line Examples

Table 5.1 - Maximum Performance at Each Bias

$|\Gamma_{LforMax}|$=0.6 Compression =1dB

Bias Point	Bias Values (V_{DS}, I_{DD})	Max Power (dBm)	Max Efficiency (%)
B1	10V, 500mA	33.3	48
B2	6V, 600mA	30.4(2dBcomp)	42(2dB comp)
B3	3V, 900mA	24.9(Γ_L=0.7)	12(Γ_L=0.7)
B4	3V, 200mA	24.2	47
B5	10V, 200mA	33.1	61
B6	8V, 300mA	31.3	54
B7	8V, 200mA	31.3	56

have been optimum when $|\Gamma_L|$ was between 0.6 to 0.8, had $|\Gamma_L|$ reduced to 0.6. This was to avoid oscillations and to guarantee the reliability of the measurement results. The optimum angle was retained. More is given on the load pull tuning method in the next section. The angles were always in the 180°±22° range. Only 1.8GHz was used during the dc bias study since it is the centre frequency.

It can be concluded from these results that a)as the bias point moves towards a higher voltage, the maximum output available power increases and, b)as it moves towards a lower current, the maximum efficiency increases. This supports general theory on transistor biassing [6,15,16].

Theory also predicts that lower noise (but also much lower power) is attained near the B4 point. The B3 point is also in a low noise area but offers a higher gain than the B4 point.

The highest linearity is produced by the class A operation at the B2 point because it has the most swing in both directions on the dynamic load line. This point produces the lowest harmonic distortion due to this linearity.

Some linearity is lost when moving toward the class AB region of B6 and B7, but the potential for efficiency increases from the theoretical 50% maximum of the B2 point. The more non-linear operation of this bias point will produce more harmonic distortion, but the key to operating an efficient single transistor power amplifier with reasonable linearity at this class AB point, is to take advantage of its efficiency, and to improve the harmonic distortion by using proper harmonic terminations.

As one moves further down the optimum load line the class B bias point is reached where the quiescent drain current is zero. Below this point the amplifier is in the class C mode. Class B and C amplifiers are more popular at frequencies below 1GHz. Above this, most are a (type of) class A [15].

Though offering more efficiency than class A amplifiers, class B and C amplifiers are much less linear and have a noise problem that is created when the transistor(s) come in and out of conduction. Single transistor class B and C amplifiers must contain a tuned circuit at the output in order to recover the fundamental and suppress the harmonics. These filters need to be properly terminated at the harmonics. Nevertheless, class C amplifiers are far too non-linear to be used where linearity is an issue.

Biassing a class B amplifier slightly towards class A produces the hybrid class AB amplifier which avoids the turn on problem. This is done in the well known complementary push pull amplifier. It is also done in single transistor amplifiers, as is targeted here. However, the class AB amplifier suggested here is biassed

further towards class A than being merely turn on. It has about 15% I_{DSS} which places it towards the more linear region.

The B3 and B4 biassing points show that the higher voltage point has a slightly higher gain and a lower efficiency. This complies with theory. Noise is not measurable in this setup. The gathered data for these two points was not very thorough because low noise levels is not studied.

5.4 - Optimum Impedance

The actual load line is established by the DC power supply and the load impedance. The dual power supply biases both the gate voltage-to establish the drain current (y-axis), and the drain voltage (x-axis). These are applied through the input and output bias tee components. Changing the DC gate voltage with the power supply will vary the output current along the vertical "static" load line shown in Figure 5.1. When the RF signal is applied to the gate, the load impedance appearing at the drain will "pull" the load line to the left to establish the "dynamic" load line, shown also in the figure.

The load line is the series of points along which the output voltage and current moves (which equates to the impedance) and is rarely a "line" in the case of a dynamic load line. It is actually close to an ellipse due to the reactive nature of the load impedance. This is illustrated by the dashed line in figure 5.1. In fact, a reactive value in the load impedance, be it capacitive or inductive, can correct for a less than optimum slope, be it too steep or too shallow, caused by the resistive portion [18]. Since, for the transistor used, the impedance is near 180°, the load line is not very elliptical because there is not a significant reactive component.

When performing load pull measurements, this combination of real and reactive values is being searched to attain the desired performance maximum. Nevertheless, a clearly defined load impedance point on the Smith chart is usually found when searching for maximum power or efficiency [18].

It is difficult to measure the actual load line (the v-i trajectory of the load) especially at microwave frequencies. When the output power has been maximized, it can be assumed that the load "line" (or trajectory) has been optimized as well.

5.5 - Impedance Tuning Method

Proper impedance tuning requires that several steps be taken to ensure accurate and repeatable results.

The system used provided impedance tuning algorithms for searching for the peak power or gain, input power sweep routines for attaining desired compression, and DC power routines for setting the DC bias points. These functions, among others, were controllable through user defined macro files which enabled the measuring and saving of results. When used it made data acquisition more convenient, organised and less error prone because the same sequence is always followed. When searching for the best compromise between power and efficiency, tuning was done "manually" with a mouse, since this compromise decision is not available as an automatic tuning option in the software used. This decision was actually not very difficult to make, for a human.

The following is an example of such a macro file.

Macro Filename = PeakComp1.MAC

```
!peak search, compression = 1dB, measure and save.
POWER 1 OFF
BIAS A -10 .2
POWER 1 ON
PEAK SOURCE
PEAK LOAD
P1DB[-20 -3 1 1]
PEAK SOURCE
PEAK LOAD
MEASURE PIN POUT GAIN EFF DCPWR V2 I2
SAVE F2C1B5P.001
```

The above sequence illustrates the tuning procedure. The steps are elaborated on below:

POWER 1 OFF - First, the RF power is turned off so that no RF signal is present when the transistor is DC biassed to the desired quiescent point.

BIAS A -10 .2 - The transistor is biassed to 10V with a drain current of 200mA. This corresponds to the B5 point. Another parameter has been previously set to ensure that the FET device is biassed in the proper manner. The gate voltage will be raised from a starting voltage of -1.5V (close enough to pinch off) until a drain current of 200mA is reached. This is done over the GPIB bus.

POWER 1 ON - The RF power is turned on at the level that the RF source it is set at. One needs to ensure that this is not a level which will damage the device. It was set at -10dBm which, due to the RF amplifier and input setup which followed, corresponded to about 16dBm at the gate of the device. This is about 3dB below the level where any compression begins.

PEAK SOURCE - The peak search algorithm, which searches for maximum gain in this case, is begun on the source side (source pull).

PEAK LOAD - The peak search algorithm searches for maximum power on the load side (load pull).

P1DB[-20 -3 1 1] - The 1dB compression point is attained. It will begin at an RF generator power of -20dBm (about 5dBm at the device) and go no higher than -3dBm (about 23dBm at the device) in 1dB steps until 1dB compression is attained.

PEAK SOURCE, and
PEAK LOAD - Another source impedance tuning (source pull) and load impedance tuning (load pull) is performed as before since the optimum source and load impedance could change with the new input and output power levels.

P1DB[-20 -3 1 1] - The input power sweep for the 1dB compression point is redone since the final power levels could have changed slightly with the new source and load impedance.

PEAK LOAD - The optimum load impedance is searched one final time in case it has changed with the latest readjustment of power.

MEASURE PIN POUT GAIN EFF DCPWR V2 I2 - These measurements are read over the GPIB system: PIN, POUT are taken from the power meter, and V2, I2 from the powe supply. The remaining items are calculated from these measurements.

SAVE F2C1B5P.001 - The results are saved in an appropriately named file, as described previously.

The basic macro file was modified each time the measurement conditions changed (i.e. a new bias point, a new compression level, etc). The filename was also changed to correspond to the results within the file. There were actually three basic macro files being modified:

Type 1) for power or efficiency searches at 1 and 2dB compression shown above;

Type 2) for power or efficiency searches at 0dB compression in which case the RF generator performs no power sweep and is set to -15dBm to attain a relatively high non compressed point. See Appendix B1 for example.

Type 3) for measurements at the reduced gamma settings ($|\Gamma|=0.6$) there are no peak searches (optimum impedance search) since the tuners are tuned to pre-determined magnitudes and angles. There may be power compression sweeps (an example is shown in Appendix B1) or fixed generator settings, depending on the required compression.

A big advantage of using automatic measurement routines is the ease in alternately performing compression and load pull which increases the certainty in finding the optimum point. And, since the same routine, which contain the same functions, are performed every time, the numerous results are more guaranteed to be consistent and repeatable. Taking note of, and ensuring the repeatability of, the RF generator level and drain current also helps in stabilizing the measurements, and is why they are tabulated.

5.6 - Optimum Impedance Tuning Problems Which Lead to the "Reduced Gamma" Settings

Problems did occur because the VSWR at the output fundamental tuner, as well as the output power of the transistor, were high, at about 10:1 and 33.5dBm respectively. This created a situation where the optimum impedance would sometimes drift to the edge of the tuning range. This is a known disadvantage in load pull design [21]. It was sometimes discovered that the transistor was oscillating. This manifested itself by an unusually high drain current. At the time, no spectrum analyser was connected at the output so there was no means of observing when the transistor was beginning to oscillate.

Operating at such a high VSWR also increases the error in the power loss of the tuner which increases the error in output power measurement [17,21]. This could make it seem as if the optimum impedance as close to the edge as possible. This in turn can cause the transistor to oscillate. When the transistor is oscillating more power appears at the output. Since there is no frequency selectivity at the power detectors, any power from DC to 18GHz is considered "good" power, so the direction of tuning during peak search routines continues towards the edge. This further increases the VSWR which further increases the error and oscillations and the system can "drift away". It follows from the rule of thumb in metrology that the ratio between the reference impedance (50Ω) and the test object should be less than or equal to 10 (VSWR≤10:1 or $|\Gamma| \leq 0.82$) [17].

When the $|\Gamma_L| \geq 0.85$ the measurements became particularly inaccurate as can be seen by the tabulated results in Appendix B having the shaded cells. Most of the time, however, the optimum impedance settled at between $|\Gamma_L| = 0.6$ to 0.8 which is common for

this transistor [14,19]. The transistor used is generally very stable but according to specifications does have an instability region at the very edge of the Smith chart at 170°, which is where the "optimum" impedance would usually drift to when "drifting away".

In view of these tuning problems, it was decided that the maximum reflection coefficient, $|\Gamma_{Lfo}|$, be reduced to 0.6. For each bias, compression and performance setting the optimum load impedance was tuned in and then the magnitude was reduced to 0.6. at the same angle. The compression was set again to ensure that the compression level was the same in both cases. The DC bias point was also verified. The RF power level and drain current would usually be lower in the reduced Γ case since the transistor is delivering less power. The source impedance was left at its optimum value since problems rarely occurred when its reflection coefficient was high, as long as it was below 0.88. There was also no plan to insert a harmonic tuner at the input, even though such setups exist.

The difference in performance between the "optimum" and the "reduced" reflection coefficient varied. The decrease in maximum power when lowering the Γ_L from optimum (0.6 to 0.8) to 0.6 is less than 1dB. The biggest decrease is where the Γ was reduced the most (disregarding results from the tables in Appendix B where $|\Gamma_L|>0.8$). The biggest decrease in peak efficiency was 3%.

This work has more to do with the changes in performance due to harmonic loading and in the development of this tuner than with the maximum performance of a power FET. Therefore reducing slightly the magnitude of the reflection coefficient in order to achieve stability of the transistor and reliability of the results is not a major issue. In fact, as long as compression is attained at any point on the Smith chart, no matter what the power and efficiency is, a study on harmonic load pull can be executed. It is, however, more satisfying to perform the harmonic load pull at the optimum

point where the maximum performance can be attained, but this is not fully possible using a 50Ω test fixture and this transistor. A quarter wave transformer can make this possible.

5.7 - Final Choice of Bias and Impedance

The final bias point chosen is B7 (8V,200mA). The final output impedance chosen is at 0.6∠174° for the load and .81∠180 for the source. These are the settings that were used for the harmonic termination study.

8V was chosen as the drain voltage because it gives a slightly lower power than 10V and made oscillations less likely. This also has the transistor operating at a lower temperature- an advantage if it is to be built on micro strip circuit where the heat sinking (dissipation) might not be as good as on a metal test fixture. This may also avoid any surprises since the temperature will be more equalised between measurement set up and final design. It is the authors experience while working with low frequency transistors that a necessary amount of reliability is gained by operating at about half the claimed output power, even with good heat sinking. This does not seem to be heresy with microwave devices, but the precaution was taken.

As shown in Table 5.2, the B7 bias point was chosen above the B6 point because it gave about 2% higher efficiency with almost the same power for the two transistor samples. 200mA is 16% I_{DSS} which is even higher than that considered an optimum bias point for single transistor power/efficiency compromise amplifier [5]. Since no spectrum analyser was available, a drain current which would guarantee a reasonably undistorted output was chosen. The same was true for compression.

Table 5.2 - B6, B7 Bias Point Comparison For Both Transistor Samples

	TRANSISTOR F (Γ_L near 0.6∠174°)			TRANSISTOR G (Γ_L near 0.6∠183°)	
	B6 (300mA)		B7 (200mA)	B6 (300mA)	B7 (200mA)
	tuning for eff	tuning for pow	tuning for pow/eff	tuning for pow/eff	tuning for pow/eff
P_o	30.4dBm	31.3dBm	31.3dBm	31.8dBm	31.9dBm
PAE	54%	53%	56%	48%	50%

As indicated, the F transistor sample had an optimum impedance at 174° and the G transistor sample had an optimum impedance at 185°. The 174° angle was chosen because it gives an overall better performance than 185° at 1.85GHz as shown in Table 5.3.

Table 5.3 - Comparison Between 174° and 185°

Trans. G	Compression = 1dB; $\lvert\Gamma_L\rvert \leq 0.6$; Bias =B7			
	$\angle\Gamma_L$=174°		$\angle\Gamma_L$=185°	
	Freq=1.8	Freq=1.85	Freq=1.8	Freq=1.85
Γ_s	.82/180°	.84/149°	.82/180°	.84/149°
Γ_L	.6/174°	.57/144°	.6/185°	.57/156°
P_o(dBm)	31.3	27.6	31.9	26.1
Eff(%)	56	21	50	20

The extra power at the periphery frequency, shown in the shaded cells, was convincing. (No retuning is done when moving between frequencies, which is the normal situation in with a fixed

termination and so observe that the terminating impedances change with frequency.)

This choice of impedance was actually done prior to the study undertaken in Section 4.3.2 for the "safest" range of the fundamental reflection angle. As seen in Figure 4.6, the recommended range of fundamental reflection angles which work well with the harmonic tuner is from 175° to 225°. Had this information been available beforehand, the optimum load impedance chosen here may have been closer to 180°. However, 174° is close enough to the "smooth" region and no problems were noticed during harmonic tuning.

Table 5.4 are the results at all frequencies at the chosen bias and impedances. The harmonic impedances are shown. These results will be used to guage the performance results of harmonic tuning.

Table 5.4 - Final Fundamental Tuning Results at the Chosen Bias and Impedance (No Multi-Harmonic Tuner Installed)

BIAS	TRANSIST SAMPLE G	F=1.75GHz		F=1.8GHz		F=1.85GHz	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V .2 A	Γ_s	.80/-148		.82/180		.84/149	
	Γ_L	.69/-152		.6/174		.58/144	
	$Z(2f_0)$	15+j20		12+j22		15+j58	
	$Z(3f_0)$	42+j40		92-j5		46-j51	
	P_i(dBm)	18.0	22.7	18	20.0	24.6	27.1
	P_o(dBm)	24.6	28.3	31.3	32.4	27.6	29.1
	Gain	6.6	5.6	13.3	12.4	3	2
	Eff(%)	12	18	56	63	22	20
	I_D(mA)	240	346	287	324	167	193
	RF GEN	-10.4	-5.8	-10.5	-8.5	-4.4	-1.6

5.8 - Conclusion

The bias point, load and source impedance has been chosen after investigating seven bias points and three performance goals. Only the two fundamental tuners were used for this study. The bias point and impedances were chosen for a compromise between power and efficiency (PAE). For the output, a compromise was also made between the transistor's stability and its maximum performance. This was accomplished by using a drain voltage 2V below the maximum (8V instead of 10V) and a magnitude of the reflection coefficient of about 0.1 lower than what would normally have been the optimum

(0.6 instead of 0.7). The reduction in the magnitude of the reflection coefficient also improves the measurement accuracy by lowering the SWR seen by the tuner and it will also accommodate the to be installed multi-harmonic tuner which will present a real loss to the reflected fundamental signal, which has the effect of reducing the maximum magnitude of the reflection coefficient provided by the fundamental tuner.

The output power and efficiency at all three frequencies were measured for 1dB and 2dB compression. These results are tabulated and will be used to guage the improvement due to harmonic tuning.

CHAPTER 6

Comparative Results

6.1 - Introduction

The multi-harmonic tuner was installed and second and third harmonic sweeps were performed in order to search for the maximum performance. The performance comparisons are tabulated.

6.2 - Installation of the Harmonic Tuner

The multi-harmonic tuner was installed and initialised. The frequency was set to 1.8GHz. The fundamental tuners were tuned in order that the load and source impedance (seen from the device) were the same as those chosen in Chapter 5 (Table 5.4): Z_L=12.9+j2.3 and Z_s=5.1-j0.2 (Γ = 0.6∠174 and 0.82∠180). The source tuner's resonator probe was thereby in the same x and y position as before and the fundamental load tuner's resonator probe was in a different position due to the insertion of a component between it and the device. The new fundamental tuner's probe would be deeper into the airline to give a higher real impedance since the harmonic tuner attenuates the reflected wave and therefore the reflection needs to be greater. The x position of the probe along the airline is different since the entire tuner is at a different distance from the device. In any case, after retuning the same impedances at the fundamental were displayed on the Smith chart.

Measurements were taken with the multi-harmonic tuner in the initialised state and are presented in Appendix C-1. These "initialized multi-harmonic tuner" results were useful in providing a performance reference when needed, such as after the setup had been broken up (i.e. after somebody "borrows" a component). The multi-harmonic tuner only needed to be initialised, not re-tuned,

to ensure that the original measurement conditions were still in effect. These results also provide a set of results at a particular set of harmonic impedances and show how the performance can decrease with harmonic tuning: the output power and PAE fell by 0.3dB and 3% respectively at a 2dB compression.

6.3 - Multi-Harmonic Optimization

Multi-harmonic load pulling was performed. The optimised results are shown in Table 6.1. Tuning was optimised at 1.8GHz.

Table 6.1 - Final Multi-Harmonic Tuning Results At 1&2dB Compression

BIAS	TRANSIST SAMPLE G	F=1.75GHz		F=1.8GHz		F=1.85GHz	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V 200 mA	Γ_s	.81/-147		.82/180		.83/149	
	Γ_L	.45/-154		.6/174		.57/150	
	Γ_2	.88/175		.91/108		.84/33	
	$Z(2f_0)$	3+j2		3.5+j36		52+j156	
	Γ_3	.84/116		.84/-35		.82/148	
	$Z(3f_0)$	6+j31		45-j145		6+j14	
	P_i(dBm)	19.6	24.6	18.5	20.5	24.5	26.8
	P_o(dBm)	27.5	31.4	31.8	32.8	27.9	29.2
	Gain	7.8	6.8	13.4	12.3	3.4	2.4
	Eff(%)	25	40	65	70	26	28
	I_D(mA)	229	341	283	322	158	160
	RF GEN	-8.9	-4.0	-10	-8.1	-4.4	-2

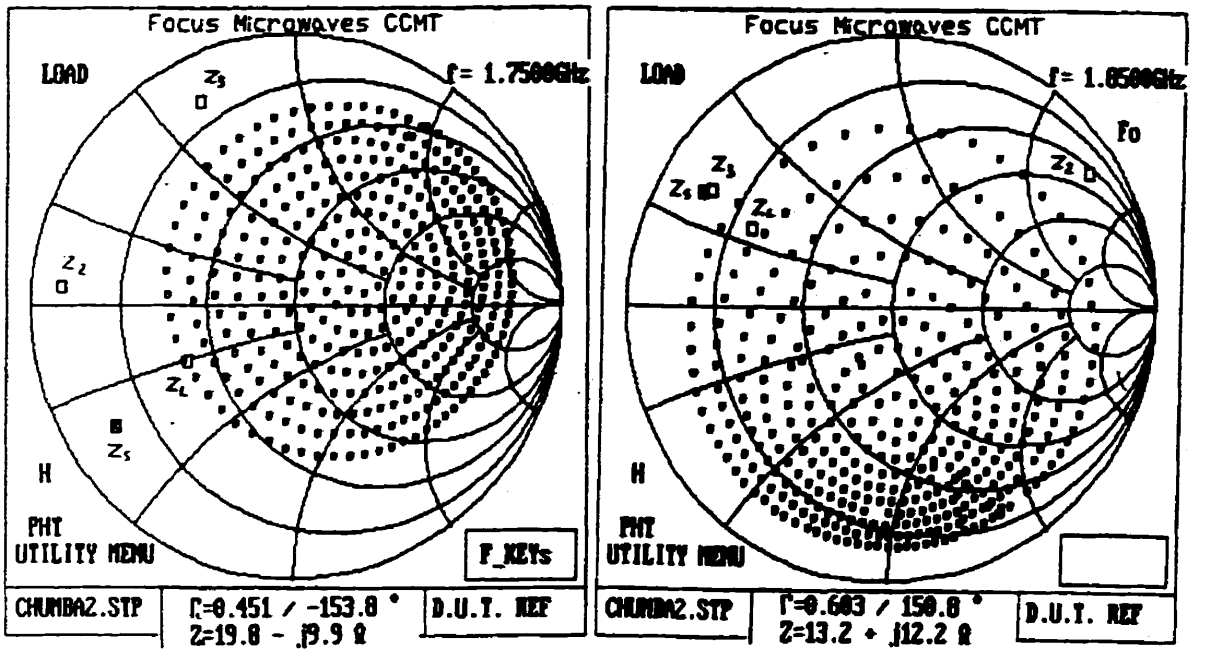
The third harmonic was swept and optimised before the second. The impedance correction utility of the fundamental and third harmonic were always enabled.

Tuning at 1.8 and 1.85GHz was successful. That is to say that the initial fundamental output impedance, Γ_L, (see Table 5.4) was attained with the new multi-harmonic tuner installed between the DUT and the fundamental tuner and tuned to the optimum harmonic impedances. A problem was encountered at 1.75GHz, the highest magnitude of the reflection coefficient, $|\Gamma_L|$, that could be attained is 0.45 as is indicated in Table 6.1 and shown by Z_L in Figure 6.1. 0.69 is needed, to attain the same value as without the multi-harmonic tuner, indicated in Table 5.4. This lack of sufficient magnitude at 1.75GHz is caused by two problems.

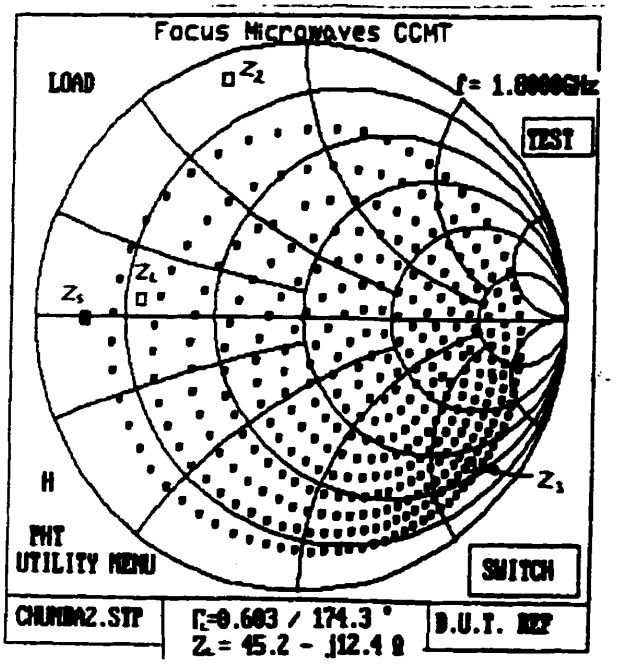
The first is simply that the multi-harmonic tuner's insertion loss reduces the maximum magnitude of the reflection coefficient possible. And, as seen in Figure 6.1, this maximum is lower for in the 1.75GHz plot than for the other two frequencies, seen by the smaller "diameter" of the calibrated points for 1.75GHz in Figure 6.1.

The second is that with all the tuners initialized the load impedance was not centred on the Smith chart (50Ω), so changing frequency results in magnitude changes. Ideally only the phase should change. In Table 5.4, when the frequency decreased to 1.75GHz, $|\Gamma_{Lfo}|$ unfortunately increased to 0.69 and now, with the multi-harmonic tuner installed, this value is unattainable especially because the maximum $|\Gamma_{Lfo}|$ is even lower in this Smith chart area due to the rotation of the calibrated points as shown in Figure 6.1. This is a situation of bad luck. At 1.8GHz and 1.85GHz, the desired fundamental impedances were attainable, as shown in the other two plots of Figure 6.1.

Due to the possibility of this problem occurring, Focus Microwaves is working to decrease the attenuation of the fundamental signal.



1.75GHz 1.85GHz



1.8GHz

Figure 6.1 - Impedance Points with the Multi-Harmonic Tuner

6.4 - Comparison of Results

The comparison of the results of the fundamental are summarised in Table 6.2. The first column are the results using only the fundamental tuners (from Table 5.4) and the second column are the final results using both the fundamental and the multi-harmonic tuner (from Table 6.1).

Table 6.2 - Comparison Between Results of Fundamental Optimization Only and Optimization Up to the Third Harmonic

F= 1.8GHz

BIAS	TRANSIST SAMPLE G	FUNDAMENTAL IMPEDANCE OPTIMIZATION ONLY		FUNDAMENTAL AND MULTI-HARMONIC OPTIMIZATION		CHANGE	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V 200 mA	Γ_s	0.82/180°		0.82/180°			
	Γ_L	0.6/174°		0.6/174°			
	Γ_2			0.91/108°			
	$Z(2f_0)$	12+j22		3.5+j36			
	Γ_3			0.84/-35			
	$Z(3f_0)$	92-j5		45-j145			
	P_i(dBm)	18	20.0	18.5	20.5	+0.5(dB)	+0.5(dB)
	P_o(dBm)	31.3	32.4	31.8	32.8	+0.5(dB)	+0.4(dB)
	Gain	13.3	12.4	13.4	12.3	+0.1	-0.1
	Eff(%)	56	63	65	70	+9	+7
	I_D(mA)	287	324	283	322	-4	-2

The comparison of the results for 1.75 and 1.85 appear in Appendix C2 and C3. The following is the summary of the improvements at each frequency.

Table 6.3 - Summary of Measured Performance Gains at Each Frequency due to Multi-Harmonic Optimisation

BIAS	TRANSIST SAMPLE G	IMPROVEMENTS AT 1.75GHz		IMPROVEMENTS AT 1.8GHz		IMPROVEMENTS AT 1.85GHz	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V 200 mA	P_i(dB)	+1.6	+1.9	+0.5	+0.5	-0.1	-0.3
	P_o(dB)	+2.9	+3.1	+0.5	+0.4	+0.3	+0.1
	Gain	+1.2	+1.2	+0.1	-0.1	+0.4	+0.4
	Eff(%)	+13	+22	+9	+7	+4	+6
	I_D(mA)	-11	-5	-4	-2	-9	-23

The 1.75GHz results can be discarded because a comparison cannot be made if the load impedance, Z_L, is different in each case. It is peculiar though, how the performance increased to such a degree with a lower magnitude of reflection coefficient.

At 1.8 and 1.85GHz the improvements are comparable, those of 1.85GHz are slightly lower. This is an expected situation since the multi-harmonic tuner is tuned for a fundamental of 1.8GHz. The most emphasis was placed on tuning at this centre frequency and the results are in the range of what has been reported[4,7].

6.5 - Performance Variations due to Second and Third Harmonic Sweeps

It is difficult at this stage of the multi-harmonic tuner development to say how much of this improvement is due to the second and third harmonic respectively. Doing a third harmonic sweep resulted in performance variances of higher than what is believed to be possible. So some of this change was probably due to fundamental and second harmonic impedance changes. It is difficult to find reliable reporting on gains due to third harmonic optimizations as "weak" to 10% has been reported [5,10,11].

The second harmonic sweep for 1dB of compression gave about a 0.6dB change in power and a 12% change in PAE (min to max). The final performance gain was 0.5 and 9% This is within reported results which are 0.4 to 1.5dB for power and 4% to 12% for PAE [4,7].

Conclusion

Fundamental and harmonic Load pull theory and systems were discussed. The fundamental automated passive load pull system was described and calibrated. The calibration and linearity was verified.

The passive automated multi-harmonic tuner was described and measured as a stand alone unit. It was then installed into the existing system and its impact was studied. Some values of the fundamental impedance did not remain constant during harmonic sweeps. These had to do with the non 50Ω impedance seen by the fundamental signal propagating through the harmonic resonators.

A 3W GaAs MESFET was load and source pulled to find the optimum fundamental source and load impedance and DC bias at 1.8GHz. The optimisation goal was to find a compromise between power and efficiency.

A final fundamental load impedance and bias point was chosen which satisfied the performance maximums of the FET and the fundamental impedance stability of the multi-harmonic tuner system. The multi-harmonic tuner was then re-installed and used to perform second and third harmonic load pull on the FET to improve on this performance. These gains were 0.5dB and 9% at the 1.8GHz fundamental for the power and power added efficiency respectively at 1dB compression. A 100MHz bandwidth was also measured by the representing 1.75GHz and 1.85GHz frequencies. A performance gain was reported at the upper frequency but at the lower frequency a high insertion loss and disadvantageous angle of the reflection coefficient in the measurement discredited the result.

This insertion loss at the fundamental had been a moderate handicap during measurements (which was possible to work around) and has pointed the development in the direction of its reduction. Thus, this work has been as much into the development of this device as it has been into harmonic tuning of transistors.

Due to the early stage of development of this device (the first device built was the one used in this study) it was difficult to attribute the performance gain specifically to the second or third harmonic. Due to the rate at which this product is developing at Focus Microwaves another study can surely follow in the near future which will be able to attribute these gains to the separate harmonics-- something which has not often been successfully done anywhere for a practical power device. It should also be possible to do this in a multi-tone environment in the PCS bands.

At that time it should be possible to perform the fundamental load pull measurements with the multi-harmonic tuner installed and initialized, since it will have a low or negligible reflection at the fundamental. It had been removed in order to attain a higher reflection coefficient.

The device should then also be installed onto a microstrip circuit, designed according to the multi-harmonic load pull findings, and then measured and compared with what has been predicted. This would validate the raison d'être of the system.

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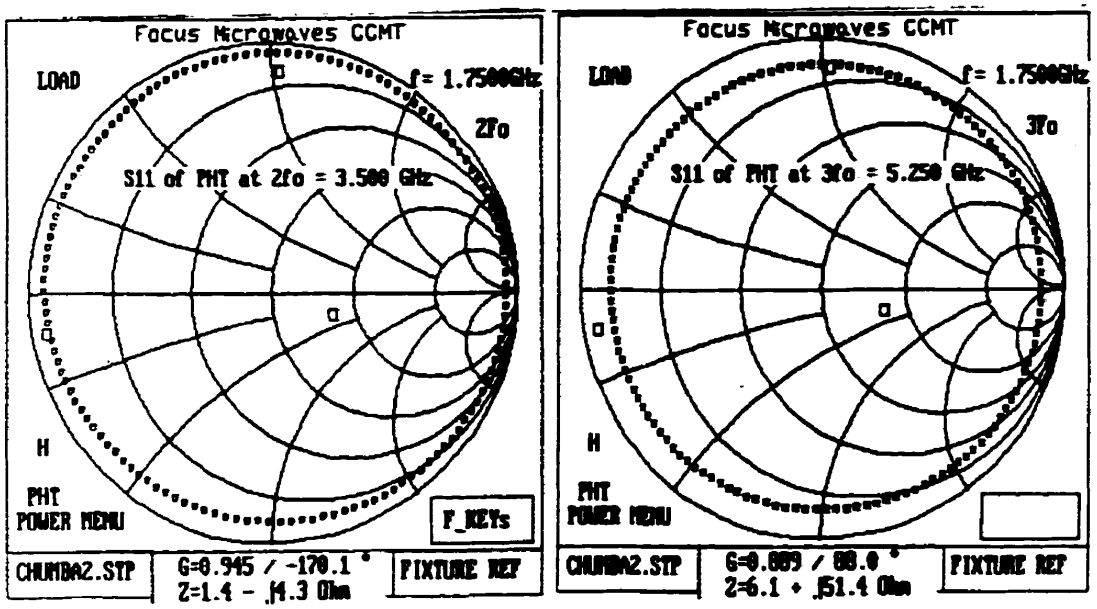
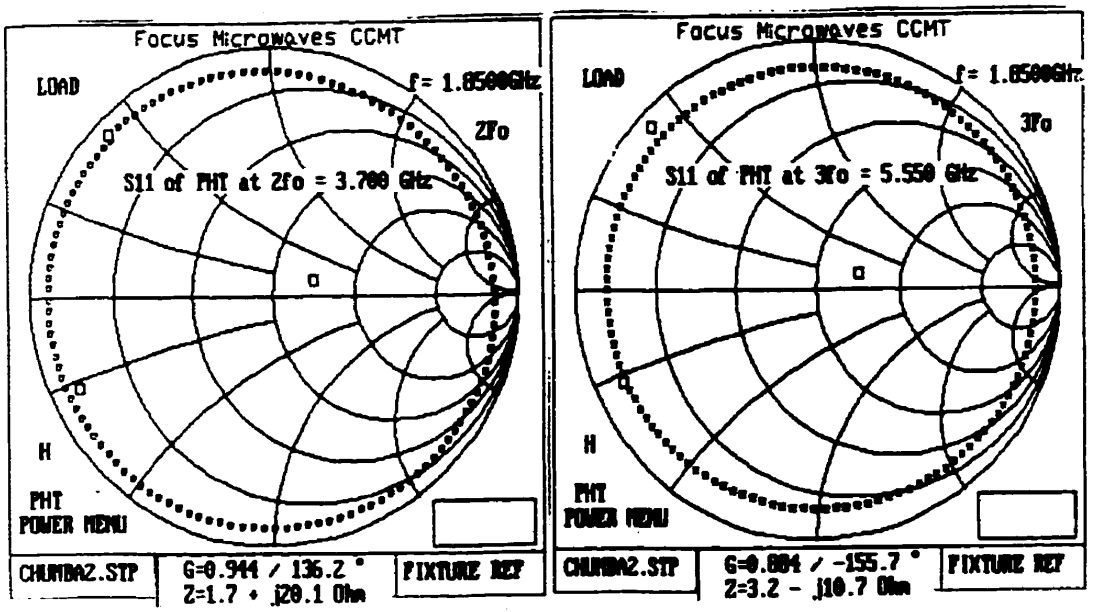
Appendix A-
Multi-Harmonic Tuner Measurements

A1 - Harmonic Impedances at Edge of Band

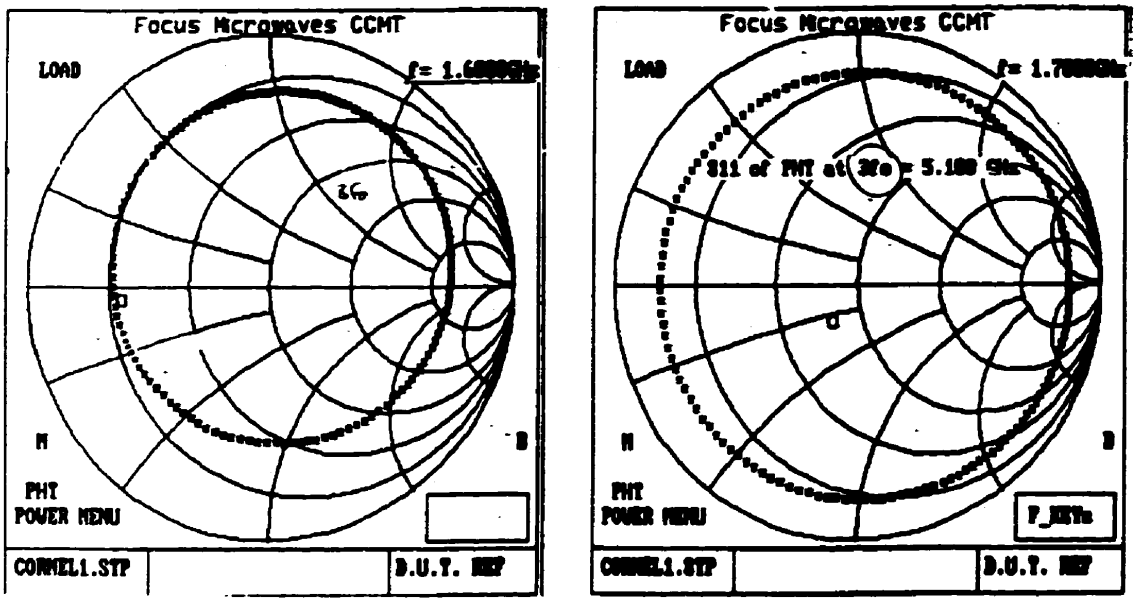


Harmonic Impedance Points at 1.75GHz

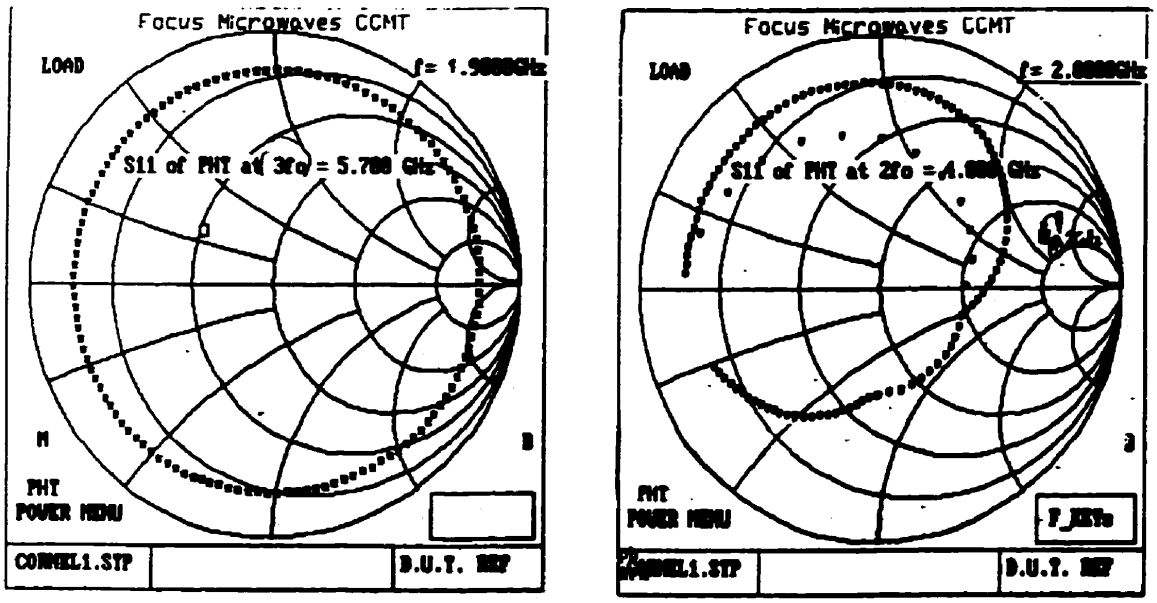


Harmonic Impedance Points at 1.85GHz

A2 - Harmonic Impedances External to Band



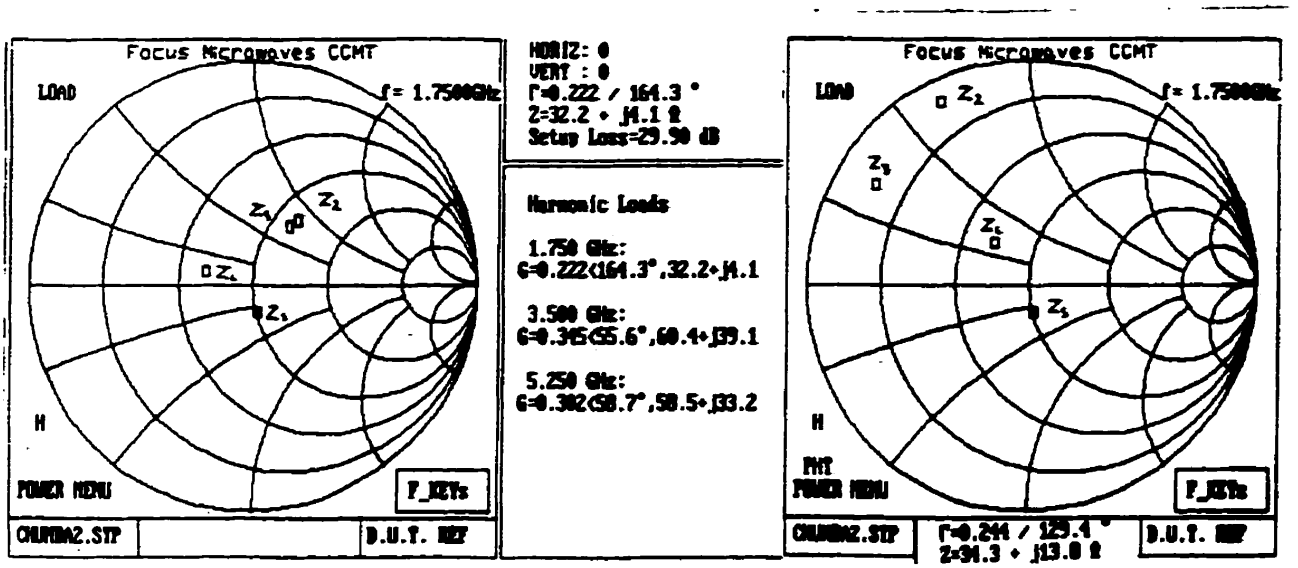
Harmonic Impedances of 1.6 and 1.7GHz



Harmonic Impedances of 1.9 and 2.0GHz

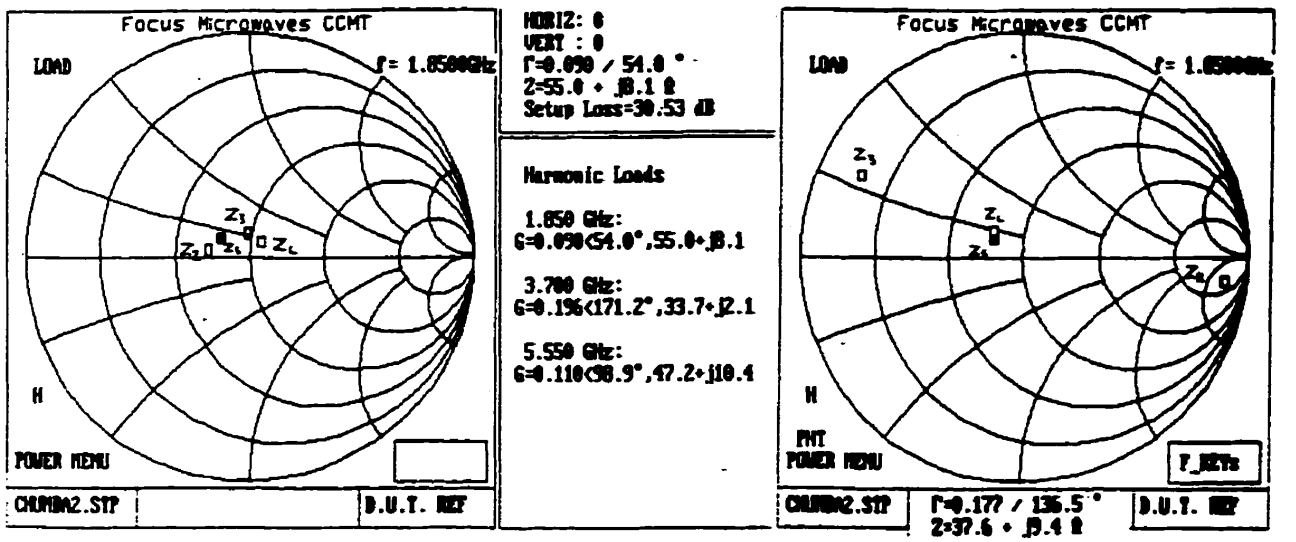
A3

Verification of Impedance before and after Multi-Harmonic Tuner Installation



Before **After**

Impedances at 1.75GHz

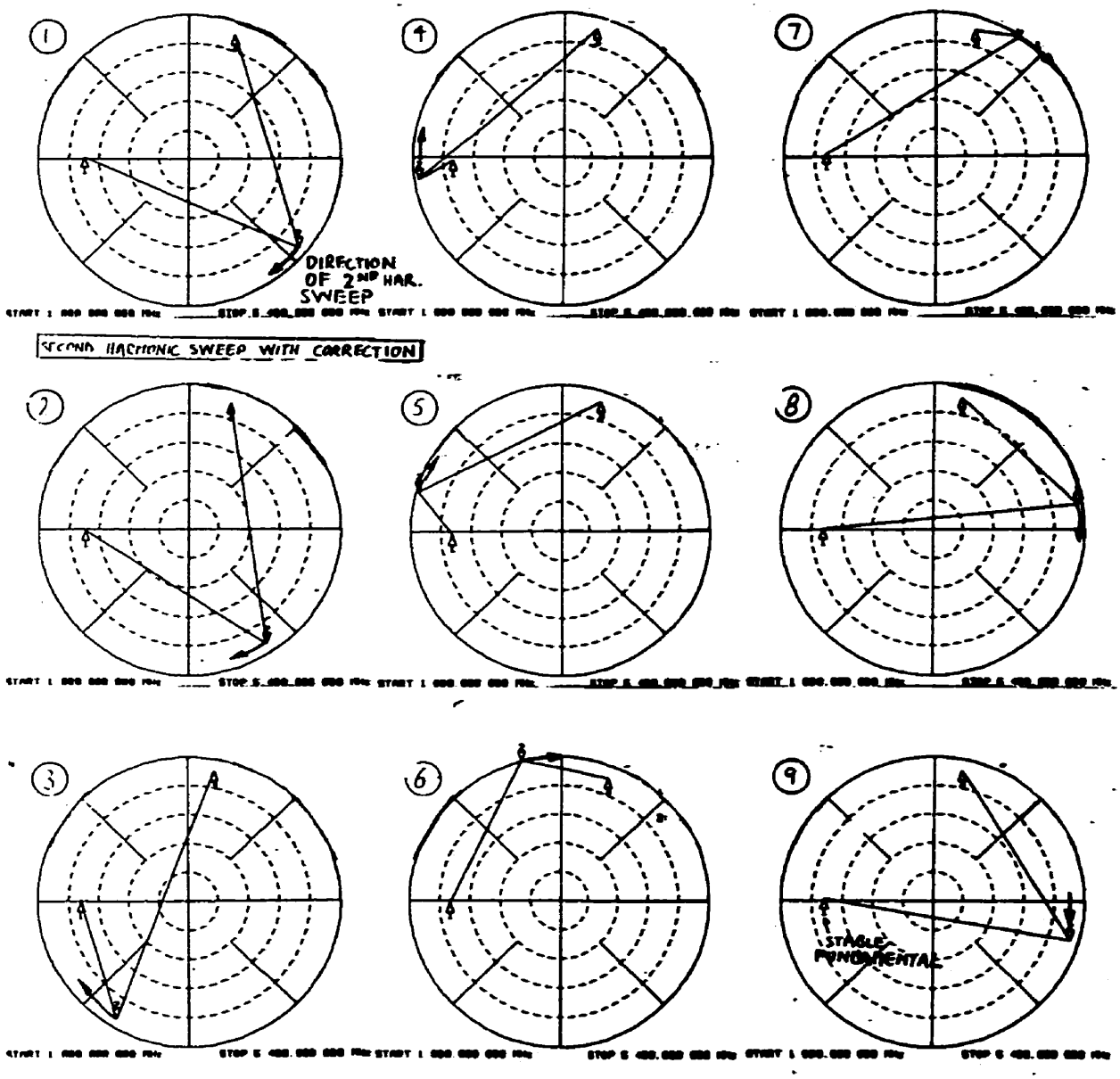


Before **After**

Impedances at 1.85GHz

A4

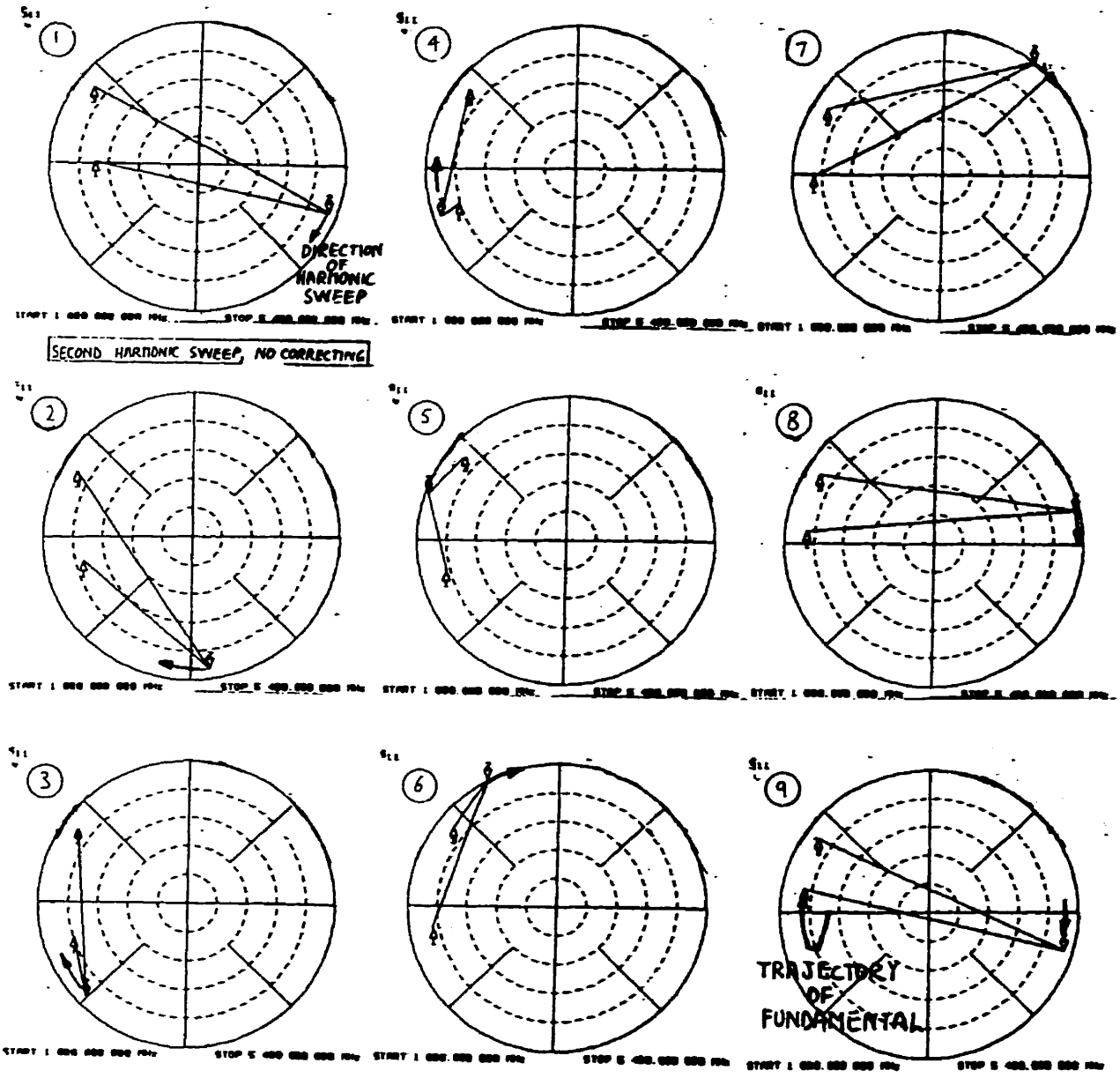
Verification of the Fundamental Impedance Stability During Harmonic Tuning Using a Network Analyser Instrument



Second Harmonic Sweep, With Correcting

A5

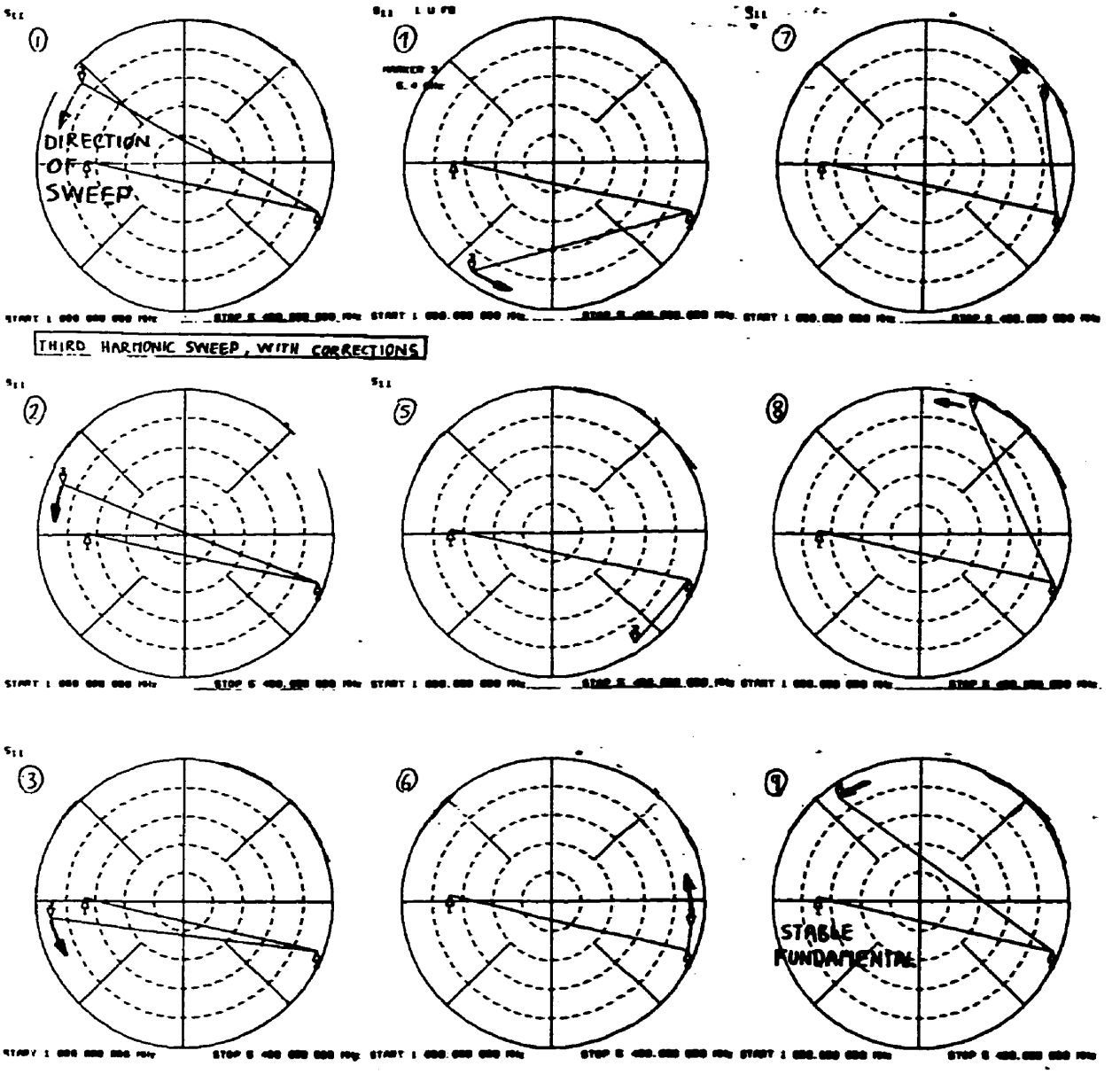
Verification of the Fundamental Impedance Stability During Harmonic Tuning Using a Network Analyser Instrument



Second Harmonic Sweep, No Correcting

A6

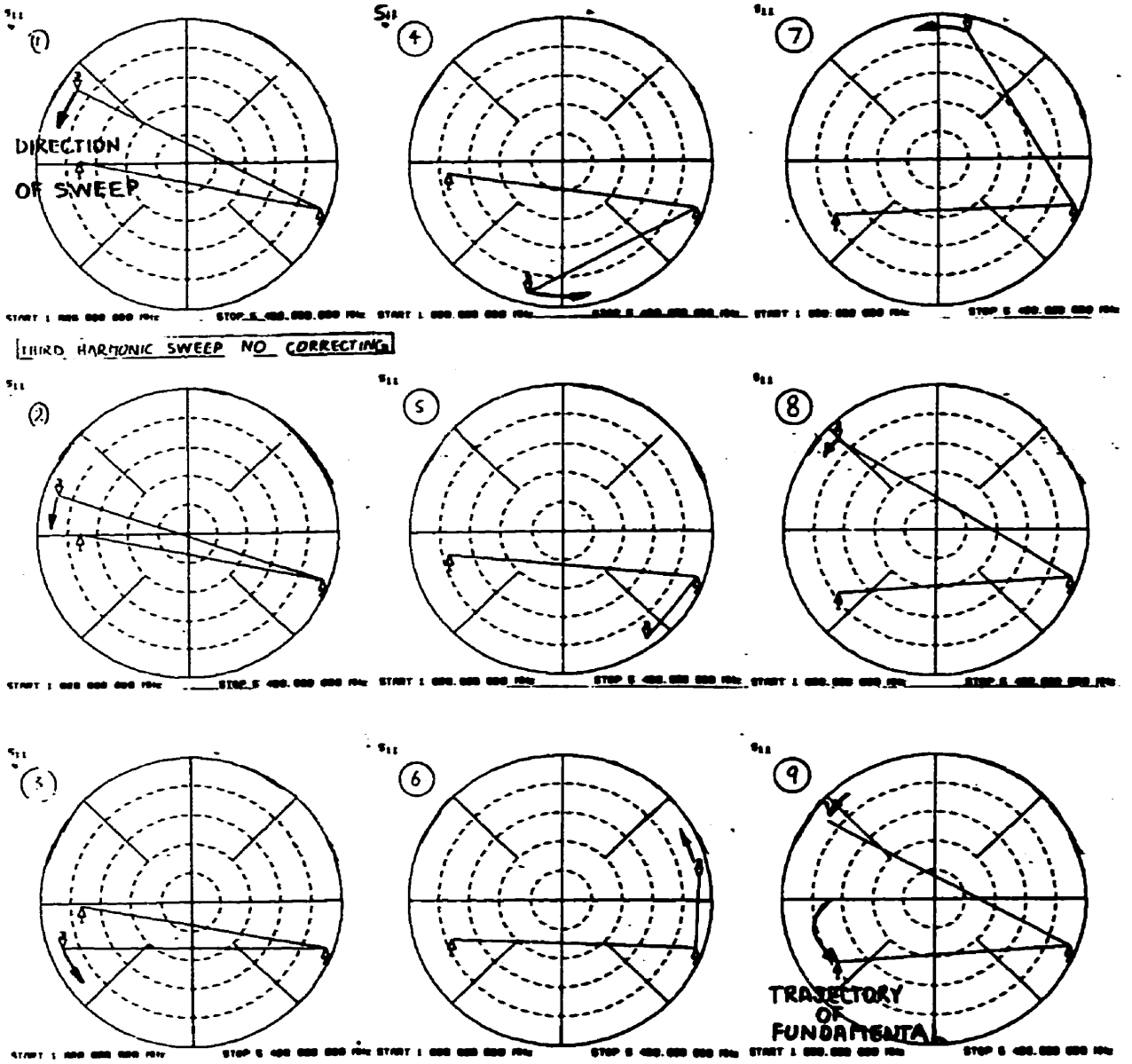
Verification of the Fundamental Impedance Stability During Harmonic Tuning Using a Network Analyser Instrument



Third Harmonic Sweep, With Correcting

A7

Verification of the Fundamental Impedance Stability During Harmonic Tuning Using a Network Analyser Instrument



Third Harmonic Sweep, No Correcting

Appendix B - Tuning Results at Various Compression Levels and Bias Points

B1

Macro File Type 2 and 3 Used For Automated Tuning and Measurement

Type 2 - Macro Filename = PinCte.MAC

```
!peak search at no compression (RF source set to give
!14/15dBm of input power), measure and save
!POWER 1 OFF
!BIAS A -10 .2
!POWER 1 ON
PSIGNAL 1 -10 0
!No compression algorithm
PEAK LOAD
PEAK SOURCE
PEAK LOAD
measure pin pout gain eff dcpwr V2 I2
save FF2C0B6P.001
```

Type 3 - Macro Filename = ReduGam.MAC

```
!Tune to reduced Gamma, meas and save
POWER 1 OFF
BIAS A -3 .3
POWER 1 ON
Tune Load g .59 -177
!No peak Search, optimum point already determined from
manual tuning
P1DB [-20 -2 1 1]
measure pin POUT gain eff DCPWR V2 I2
save G2C1B6PR.001
```

B2

Table B1 - Bias Point 1: 10V, 500mA

BIAS	COM-PRESSION	C=0dB (Pi=14dBm)		C=1dB		C=2dB	
	PARA-METERS	Optimum Load Impedance (Γ is free)					
		Eff pk	Pow pk	Eff pk	Pow pk	Eff pk	Pow pk
B1: 10V .5A	Γ_{Lfo}		.7/169	.68/167	.61/176	.61/174	.7/174
	P_o(dBm)		31.6	33.1	33.4	33.9	33.5
	Gain		17.6	15.5	16.0	15.1	16.7
	Eff(%)		31.6	49.8	45.6	55.3	47.2
	Fig #			Rep4-9	Rep4-4	Rep4-10	
	File		FF2C0B1P	FF2C1B1E	FF2C1B1P	FF2C2B1E	FF2C2B1P
		Reduced Gamma (Γ<.6) Load Impedance					
	Γ_{Lfo}		.6/169	.58/173	.58/179		.6/174
	P_o(dBm)		31.3	33.4	33.3		33.2
	Gain		17.3	15.8	16.0		16.5
	Eff(%)		29.1	48.2	44		46.8
	Fig #			Rp4-12	Rp4-5		
	File		FF2C0B1R		FF2C1B1R		FF2C2B1R

Explanation of Abbrieviations:

Eff pk - Results of this entire column have been tuned for maximum efficiency

Pow pk - Results of this entire column have been tuned for maximum power

Fig # - As per reference [22]

File - File in which these results are stored. See section 5.2

B3

Table B2 - Bias Point 2: 6V, 600mA

		COMPRESSION					
BIAS		C=0dB (Pi=15dBm)		C=1dB		C=2dB	
		Eff pk	Pow pk	Eff pk	Pow pk	Eff pk	Pow pk
	PARA-METER	Optimum Load Impedance					
B2: 6V 6A	Γ_{Lfo}					.7/173	.69/179
	P_o(dBm)						
	Gain						
	Eff(%)						
	Fig #					Rep4-15	Rep4-15
	File						
		Reduced Gamma (Γ<.6) Load Impedance					
	Γ_{Lfo}					.58/173	
	P_o(dBm)					30.4	
	Gain					15.3	
	Eff(%)					42	
	Fig #					Rep4-14	
	File						

B4

Table B3 - Bias Point 3: 3V, 900mA

BIAS		COMPRESSION					
		C=0dB (Pi=15dBm)		C=1dB		C=2dB	
		Eff pk	Pow pk	Eff pk	Pow pk	Eff pk	Pow pk
	PARA-METER	Optimum Load Impedance					
B3: 3V .9A	Γ_{Lfo}				.69/-169	.69/-175	.78/-166
	P_o(dBm)				24.9		
	Gain				15.3		
	Eff(%)				11.8		
	Fig #				Rep4-17	Rep4-18	Rep4-18
	File				FFCC1B3P		
		Reduced Gamma (Γ<.6) Load Impedance					
	Γ_{Lfo}						
	P_o(dBm)						
	Gain						
	Eff(%)						
	Fig #						
	File						

B5

Table B4 - Bias Point 4: 3V, 200mA

BIAS		COMPRESSION					
		C=0dB (Pi=2.5dBm)		C=1dB		C=2dB	
		Eff pk	Pow pk	Eff pk	Pow pk	Eff pk	Pow pk
	PARA-METER	Optimum Load Impedance (Γ is free)					
B4: 3V 2A	Γ_{Lfo}		.8/176			.87/-165	.87/-175
	P_o(dBm)		19.7			26	25.0
	Gain		17.2			19.7	15.6
	Eff(%)		16.2			-99	73?
	Fig #		Rep4-19			Rep4-21	Rep4-20
	File					FF2C2B4E	FF2C2B4P
		Reduced Gamma (Γ<.6) Load Impedance					
	Γ_{Lfo}				.59/-174		.59/-174
	P_o(dBm)				24.2		25
	Gain				15.1		14.1
	Eff(%)				47.2		54.4
	Fig #				Rep4-20		Rep4-22
	File						

B6

Table B5 - Bias Point 5: 10V, 200mA (Class AB)

BIAS		COMPRESSION					
		C=0dB (Pi=2.5dBm)		C=1dB		C=2dB	
		Eff pk	Pow pk	Eff pk	Pow pk	Eff pk	Pow pk
	PARA-METER	Optimum Load Impedance					
B5: 10V 2A	GAMMA	.7/160	.87/175.	.7/158	.7/176	.61/174	.7/177
	Pi(dBm)	14.8	14.9	17.0	19.7	19.9	20.6
	P_o(dBm)	31.2	32.9	31.2	35.0	34.6	34.9
	Gain	16.3	18.1	14.2	15.3	14.7	14.3
	Eff(%)	57.1	39.4	60.8	58.6	59.9	57.1
	File		FF2C0B5P		FF2C1B5P		FF2C2B5P
		Reduced Gamma (Γ<.6) Load Impedance					
	GAMMA	.6/160	.6/175	.59/157	.60/178	.60/173	.60/174
	P1(dBm)	14.8	14.9	17.4	17.4	20.1	20.0
	P_o(dBm)	31.0	31.5	31.6	33.1	34.7	34.8
	Gain	16.1	16.7	14.2	15.7	14.6	14.9
	Eff(%)	53.9	46.7	60.8	52.4	59.6	59.7
	File		FF2C0B5R		FF2C1B5R		FF2C2B5R

B7

Table B6 - Bias Point 6: 8V,300mA (Transistor Sample F)

BIAS	Freq=1.8GHz	COMPRESSION (dB)					
		C=0dB (Prf=-9.5dBm)		C=1dB		C=2dB	
		Eff pk	Pow pk	Eff pk	Pow pk	Eff pk	Pow pk
	PARA-METER	Optimum Γ					
	Γ_s	.88/176	.88/176	.82/180	.88/178	.82/-179	.83/-179
B6 8V 3A	Γ_L	.7/165	.8/176.5	.7/162	.8/176	.81/160	.7/177
	P_i(dBm)	14.5	14.6	14.6	16.1	17.7	16.4
	P_o(dBm)	30.4	31.3	30.0	31.7	30.9	32.5
	Gain	15.8	16.8	15.3	15.7	13.2	16.1
	Eff(%)	53.4	44.7	53.0	47.1	45.0	42.3
	I_D(mA)	241	375	228	387	325	420
	File	F2C0B6E	F2C0B6P	F2C1B6E	F2C1B6P	F2C2B6E	F2C2B6P
		Deliberately Reduced $\|\Gamma\|$ ($\|\Gamma_L\|$<.6)					
	Γ_s	.88/176	.88/176	.82/180	.88/178	.82/-179	.88/178
	Γ_L	.6/165	.6/177	.6/162	.6/176	.6/160	.6/177
	P_i(dBm)	14.5	14.6	15.2	15.9	17.0	16.4
	P_o(dBm)	30.1	30.6	30.4	31.3	31	31.6
	Gain	15.6	16.0	15.2	15.4	14.0	15.2
	Eff(%)	50.2	47.7	53.7	52.5	63	53
	I_D(mA)	251	296	246	312	243	332
	File	F2C0B6ER	F2C0B6PR	F2C1B6ER	F2C1B6PR	F2C2B6ER	F2C2B6PR
		C=0dB		C=1dB		C=2dB	
		COMPRESSION (dB)					

B8

Table B7 - Bias Point6: 8V, 300mA (Transistor Sample: G)

BIAS	Freq=1.8GHz	COMPRESSION					
		C=0dB		C=1dB		C=2dB	
		Eff pk	Pow pk	Eff/Pow	Pow pk	Eff/Pow	Pow pk
	PARA-METER	Optimum Γ					
	Γ_s				.88/-177		.88/-177
B6 8 V .3A	Γ_L				.80/-177		.87/-170
	P_i(dBm)				19.0		18.2
	P_o(dBm)				33.9		34
	Gain				14.9		15.8
	Eff(%)				52.3		44.9
	I_D(mA)				562		683
	File				G2C1B6P		G2C2B6P
		Deliberately Reduced $\|\Gamma\|$ (Γ_L<.6)					
	Γ_s			.81/-177	.88/-177	.82/-178	
	Γ_L			.60/-175	.60/-177	.60/172	
	P_i(dBm)			18.2	17.8	20.0	
	P_o(dBm)			31.8	32.3	32.6	
	Gain			13.6	14.5	12.5	
	Eff(%)			48	52.7	63.4	
	I_D(mA)			381	389	335	
	File			G2C1B6BR	G2C1B6PR	G2C2B6BR	
		C=0dB		C=1dB		C=2dB	
		COMPRESSION (dB)					

Eff/Pow- Results of this entire column have been manually tuned for a compromise between maximum efficiency and maximum power

B9

Table B8 - Fundamental Tuning Results at Various Frequencies
Bias Point 7: 8 V, 200 mA, Fund. Only
(Transistor Sample: G)

BIAS		COMPRESSION = 1dB			
		Γ_1 = 0.6/174°		Γ_2 = 0.6/-175	
		f=1.8	f=1.85	f=1.8	f=1.85
	PARA-METER	Reduced Gamma (Γ<.6) Load Impedance			
B7 8V .2A	Γ_s	.82/180	.84/149	.82/180	.84/149
	Γ_L	.6/174	.57/144	.6/-175	.57/156
	P_i(dBm)	17.9	24.7	18.5	21.8
	P_o(dBm)	31.3	27.6	31.9	26.1
	Gain	13.4	2.9	13.4	4.3
	Eff(%)	56.0	21.0	50.4	19.8
	I_D(mA)	286	165	366	163
	RFSourc	-10.3	-4.0		

Appendix C - Comparison of Results

C1

Table C1

Tuning Results at 1&2 dB Compression

(Multi-harmonic Tuner Installed and Initialised)

BIAS	TRANSIST SAMPLE G	F=1.75GHz		F=1.8GHz		F=1.85GHz	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V 200 mA	Γ_s	.81/-147		.82/180		.84/149	
	Γ_L	.63/-157		.6/174		.59/144	
	Γ_2	.92/116		.92/56		.88/-7.3	
	$Z(2f_0)$	3+j31		10+j93		395+j395	
	Γ_3	.84/147		.84/-22		.8/153	
	$Z(3f_0)$	5+j15		102-j212		6+j12	
	P_i (dBm)	19	26.3	18.5	20.2	24.5	27.0
	P_o (dBm)	26.4	32.7	31.5	32.1	27.9	29.3
	Gain	7.4	6.4	13	12	3.4	2.3
	Eff(%)	18	38	59	60	26	24
	I_D (mA)	253	472	282	317	158	179
	RF GEN	-9.5	-1.8	-10	-8.4	-4.4	-1.7

C2

Table C2 - Comparison of Results at 1.75GHz

BIAS	TRANSIST SAMPLE G	FUNDAMENTAL IMPEDANCE OPTIMIZATION ONLY		FUNDAMENTAL AND MULTI-HARMONIC OPTIMIZATION		CHANGE	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V 200 mA	Γ_s	.80/-148		.81/-147			
	Γ_L	.69/-152		.45/-154			
				.88/175			
	$Z(2f_0)$	15+j20		3+j2			
				.84/116			
	$Z(3f_0)$	42+j40		6+j31			
	P_i(dBm)	18.0	22.7	19.6	24.6	+1.6(dB)	+1.9(dB)
	P_o(dBm)	24.6	28.3	27.5	31.4	+2.9(dB)	+3.1(dB)
	Gain	6.6	5.6	7.8	6.8	+1.2	+1.2
	Eff(%)	12	18	25	40	+13	+22
	I_D(mA)	240	346	229	341	-11	-5

C3

Table C3 - Comparison of Results at 1.85GHz

BIAS	TRANSIST SAMPLE G	FUNDAMENTAL IMPEDANCE OPTIMIZATION ONLY		FUNDAMENTAL AND MULTI-HARMONIC OPTIMIZATION		CHANGE	
		COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB	COMP=1dB	COMP=2dB
#7 8V 200 mA	Γ_s	.84/149		.83/149			
	Γ_L	.58/144		.57/150			
				.84/33			
	$Z(2f_0)$	15+j58		52+j156			
				.82/148			
	$Z(3f_0)$	46-j51		6+j14			
	P_i(dBm)	24.6	27.1	24.5	26.8	-0.1(dB)	-0.3(dB)
	P_o(dBm)	27.6	29.1	27.9	29.2	+0.3(dB)	+0.1(dB)
	Gain	3	2	3.4	2.4	+0.4	+0.4
	Eff(%)	22	20	26	28	+4	+6
	I_D(mA)	167	193	158	160	-9	-23